MACROMODEL OF CMOS CCII WITH NONLINEAR AND NOISE PARAMETERS

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Abstract – **A macromodel of second generation current conveyor (CCII) has been proposed. The model allows simulation of CCII frequency response, their noise and weakly nonlinear properties. The frequency dependencies of CCII transfer coefficients have been taken into account by means of inclusion to the macromodel of resonant- and RC-circuits. The nonlinear properties were described using nonlinear controlled sources, while the noise properties were described by two current and one voltage equivalent noise sources connected to CCII terminals. An accuracy of the proposed model has been verified by computer simulation and comparison of the results with simulation on the transistor level and experimental data.**

Index terms – **current conveyor, macromodel, computer simulation, CMOS, filter design, noise, nonlinear properties.**

I. Introduction

In modern communication systems (such as WLAN, DECT and Bluetooth) the use of filters with improved frequency properties is necessary. At the same time, the design of so called zero-IF Receivers makes it possible to avoid the realization of the system with external bandpass filters, because these blocks can be replaced by chip-internal CMOS low-pass filters with cut-off frequency equal to 1MHz and higher. A possible way to design these filters is a switched-capacitor (SC) technique. There is a serious problem in design of discrete-time circuits. It is a long time of computer simulation. For example, when active components are presented in the transistor level only the measuring of the AC response of 5^{th} order low-pass filter may take about 1-2 days. Taking into account that harmonic and noise characteristics should be obtained as well, it is possible to conclude that complete simulation process of the discrete circuits takes a lot of machine time. Therefore to accelerate the process of the filter design accurate macromodels of active elements are needed.

High-frequency filters with small chip area and low power consumption can be synthesized using the combination of second generation current conveyors (CCII) and SC technique [1]. This approach gives an opportunity to realize filters with high frequency- and dynamic ranges. Unfortunately, by now very few papers with current conveyor macromodels have been published [2], [3]. In these papers linear and nonlinear macromodels of CCII have been proposed. The comparison of the characteristics of macromodel with respective parameters of transistor level model of CCIIs was performed. It had proven the accuracy of proposed macromodel. Moreover, there are not any papers with CCII macromodels where the noise properties had been taken into account. However, the noise equivalent circuit of CCII is known [4], [5].

Thus, the purpose of the current paper is to develop the macromodel of the second generation current conveyor where the frequency, nonlinear and noise characteristics are described accurately. This macromodel must be suitable for the simulation of the CCII-based high-frequency SC-filters.

The paper is organized as follows: after the Introduction the linear model of CCII is described in Section II. This Section includes idealized presentation of the block as well as the model taken into account CCII frequency properties. In Section III the nonlinear properties of current conveyors are considered and respective additions are included to the model. The Section IV is devoted to the noise characteristics of CCIIs. In this Section the principles of noise analyses of CCIIs are discussed and the equivalent noise sources are added to the macromodel. In Section V the computer simulation of obtained macromodel is carried out and the comparison with the results of transistor level simulations and the results of measurements of test CMOS chips is considered. The Section VI is Conclusion where the results of the paper are summarized.

II. Linear model of CCII

On the first step of the filter design the idealized model of the using active elements can be needed. In the case of the CCII the idealized model, based on representation proposed in [6, p.121], consists of one voltage controlled voltage source (VCVS), one current controlled current source (CCCS) and three resistors as shown in Fig. 1. It is necessary to note that, depending on type of CCII, the gains of VCVS and CCCS are equal to 1 and ±1 respectively, the resistances of resistors R_Z and R_Y tend to infinity and the resistance of R_X tends to zero for an ideal case. To avoid the singular matrix problem during the analysis and simulation it is rationally to keep the resistances of R_Z and R_X as finite values.

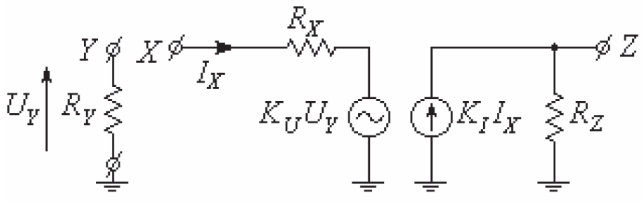

Fig. 1: Idealized model of CCII.

When the frequency properties of current conveyors have to be taken into account only three capacitors between analog ground and other terminals of the current conveyor allows the description of the frequency behavior with sufficient accuracy. However, there are cases when the AC response of the CCII has the resonance pick. In that case the inductor should be included to the macromodel. As a result the resonant circuit will be formed at *X*-terminal (see Fig. 2). The *Q*-factor of resonant circuit is regulated by additional resistor R_p.

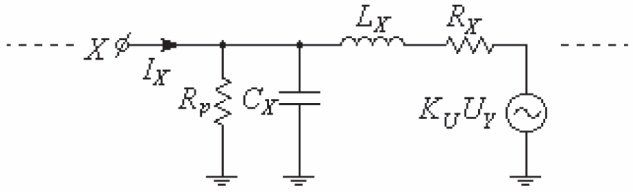

Fig. 2: The resonant circuit at *X*-terminal.

It is appropriate mention here that in macromodel proposed in [2], [3] an additional block is used to limit the current at *X*-terminal when this terminal is shorted to ground. But if CCII is used in circuits where such a situation is impossible this block can be omitted.

III. Nonlinear model of CCII

In [2], [3] the nonlinear behavior of the CCII is modeled by the diode limiters. This is a correct method but on this way we shall have some difficulties. First, the diode is comparatively complex semiconductor device and in the most of simulation programs it presents by its own macromodel. It leads to increase of the time of simulation. Second, for each circuit of CCII the individual specifications of diode parameters are needed.

Therefore now we would like to propose another approach in nonlinear properties modeling. It is based on mathematical description of the nonlinear element by truncated power series because computer simulation programs allow the using of mathematical formulas in description of dependent sources. As an example of the using of such sources we would like to demonstrate the realization of nonlinear VCVS. Let us assume that the input voltage signal is of harmonic type $u_{in} = U_{in0} \cdot \cos(\omega_0 \cdot t)$ and effects of second and third orders should be taken into account. The amplitudes of 1st, 2nd and 3rd harmonic components of output signal are supposed to be known and equal to U_1, U_2 and U_3 respectively. Further, the output signal u_{out} is described by the following equation

$$u_{out}(u_{in}) = a_0 + a_1 u_{in} + a_2 u_{in}^2 + a_3 u_{in}^3, \quad (1)$$

where $a_0 = -\frac{U_{in0}^2}{2} \cdot a_2$ corresponds to additional DC shift that can be added to offset voltage at *X*-terminal. Substituting the sinusoidal input signal to equation (1) and performing the trigonometric transformations we can obtain the next system of linear equations

$$\begin{cases} \frac{U_{in0}^3}{4} \cdot a_3 = U_3 \\ \frac{U_{in0}^2}{2} \cdot a_2 = U_2 \\ \frac{3U_{in0}^3}{4} \cdot a_3 + U_{in0} \cdot a_1 = U_1 \end{cases}$$

After the solving of this system relative to a_1, a_2 and a_3 values of the coefficients of the polynomial will be obtained. It should be noted that in the case of a balanced circuit the even harmonic components would not be taken into account. Therefore in such a case the polynomial may has the following form

$$u_{out}(u_{in}) = a_1 u_{in} + a_3 u_{in}^3.$$

The distortion of current at *Z*-terminal can be performed analogously.

IV. Noise model of CCII

Before the modeling of the noise properties of CCIIs let us consider an equivalent noise circuit of current conveyor discussed in [4], [5]. In these papers an equivalent noise circuit for current conveyor with multiple *Z*-terminal has been proposed. But for the single *Z*-terminal CCII the noise circuit can be simplified. It consists of two current noise sources and one voltage noise source shown in Fig. 3.

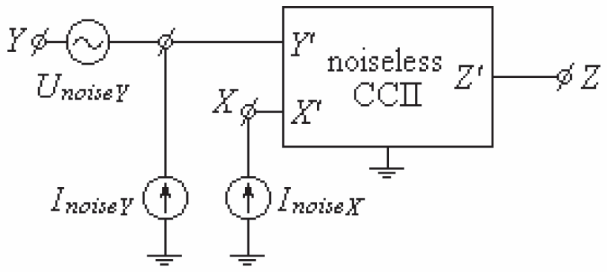

Fig. 3: Noise model of CCII.

It is important to note that in the most of structures of CMOS current conveyors the *Y*-terminal is connected to the gate of MOS-transistor. In this case the value of noise current at *Y*-terminal (I_{noiseY}) may be neglected.

The approach of calculation of values of equivalent noise current at *X*-terminal and equivalent noise voltage at *Y*-terminal is as follows. First, the equivalent circuit of transistor-level CCII for AC and nodal equations for this circuit are formed. The voltage is transferred from *Y*-terminal to *X*-terminal of CCII with gain K_U equal to 1. Therefore to obtain the value of noise voltage at *Y*-terminal (voltage input) it is possible to determine the noise voltage at *X*-

terminal (voltage output) solving the linear set of nodal equations and recalculate it to *Y*-terminal using equation (2).

$$U_{noiseX} = K_U U_{noiseY} \quad (2)$$

To calculate full noise voltage in *X*-terminal it is necessary to define the noise voltage in this terminal when only one noise source, for instance $\overline{I_i^2}$, in the circuit is taken into account while the other current noise sources have been excluded from the circuit. Let us call the voltage claimed at *X*-terminal by an operating noise source as $\overline{U_i^2} = |z_i|^2 \overline{I_i^2}$, where z_i is transimpedance from the *i*-th source to *X*-terminal. This procedure has to be performed for each of *N* noise sources by turns (usually the value of *N* is equal to number of transistors in the circuit). After that the RMS noise voltage at *X*-terminal may be obtained by means of superposition principle assuming an independence of noise sources. Thus an equivalent voltage noise source at *X*-terminal is determined as

$$\sqrt{\overline{U_{noiseX}^2}} = \sqrt{\sum_{i=1}^{N} \overline{U_i^2}}$$

The value of equivalent noise current source at *X*-terminal is calculated by the same manner. The current gain k_i from each of *N* noise sources to *Z*-terminal must be defined when *Y*-terminal is grounded. The RMS noise current at *Z*-terminal is calculated by following equation

$$\sqrt{\overline{I_{noiseZ}^2}} = \sqrt{\sum_{i=1}^{N} |k_i|^2 \cdot \overline{I_i^2}} .$$

As an example let us demonstrate the results of noise analyses of CCII used in filter considered in [1] (see Fig.4).

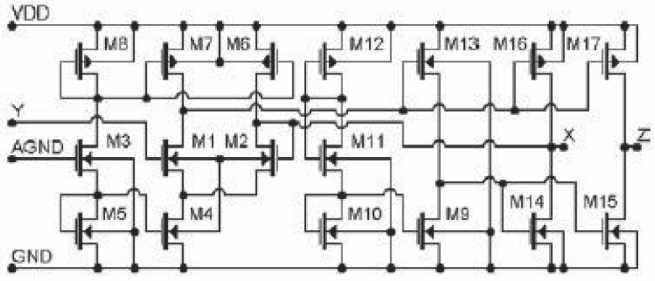

Fig. 4: CCII based on differential cascade [1]

Assuming that
$W1/L1=W2/L2=W3/L3$,
$W6/L6=W7/L7=W8/L8=W12/L12$,
$W9/L9=W10/L10=W11/L11=W13/L13$,
$W14/L14=W15/L15$, $W16/L16=W17/L17$
the noise voltage at *X*-terminal is described by the next formula

$$\overline{U_{noiseX}^2} = \frac{4 \cdot (\overline{I_7^2} + \overline{I_8^2})}{g_{m1}^2} + \frac{\overline{I_1^2} + \overline{I_2^2} + \overline{I_4^2}}{g_{m1}^2} +$$

$$+ \frac{(2g_{m3} + g_{m4})^2 \cdot (\overline{I_3^2} + \overline{I_5^2})}{g_{m1}^2 \cdot (g_{m3} + g_{m5})^2},$$

where the numbering of noise currents corresponds to the numbering of transistors and g_{mi} is transconductance of transistor number *i*. Noise sources are described as $\overline{I_i^2} = \frac{8kT}{3} g_{mi} df$, where *k* is the Boltzmann constant, *T* is absolute temperature and *df* is the considered frequency bandwidth. The flicker noise may be taken into account if necessary but it matter in low frequencies only.

The noise current at *Z*-terminal is

$$\overline{I_{noiseZ}^2} = \overline{I_4^2} + \overline{I_6^2} + \overline{I_7^2} + \overline{I_{14}^2} + \overline{I_{15}^2} + \overline{I_{16}^2} + \overline{I_{17}^2} +$$

$$+ \frac{(g_{m4} - 2g_{m5})^2 \cdot \overline{I_3^2}}{(g_{m3} + g_{m5})^2} + \frac{(2g_{m3} + g_{m4})^2 \cdot \overline{I_5^2}}{(g_{m3} + g_{m5})^2}$$

Comparison with simulated results will be presented in the Section V.

V. Computer simulation and comparison

The complete macromodel of current conveyor is shown in Fig. 5, where functions f_U and f_I describe nonlinear VCVS and CCCS.

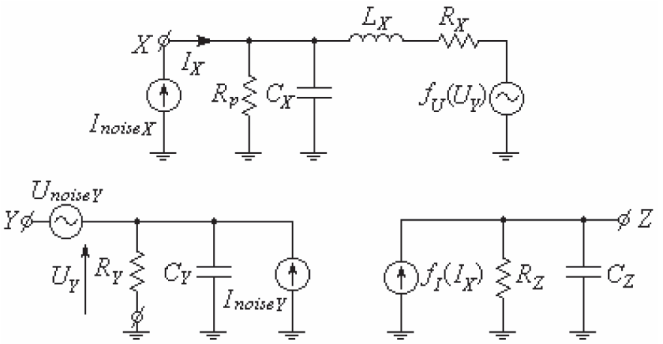

Fig. 5: The complete macromodel of CCII.

To show an accuracy of proposed macromodel it is rationally to compare the results of macromodel-level simulation with results of transistor-level simulation and experiment. In Fig. 6 the result of AC response measure of voltage gain K_U of CCII depicted in Fig. 4 is presented. In the next Fig. 7 the result of macromodel-level simulation is shown. The element values are C_X=1.5pF, L_X=2.5mH, R_p=50kΩ.

To calculate the coefficients a_i from equation (1) the harmonic signal with frequency equal to 1MHz and 1V pick-to-pick magnitude is given to *Y*-terminal of transistor-level model of CCII shown in Fig. 4. The amplitudes of 1st, 2nd and 3rd harmonics in output signal at *X*-terminal are as follows: U_1=509mV, U_2=998μV and U_3=132.4μV. Using the method described in Section III the coefficients of polynomial are defined and have the next values: a_1=1.015, a_2=7.984•10^{-3}, a_3=4.237•10^{-3}.

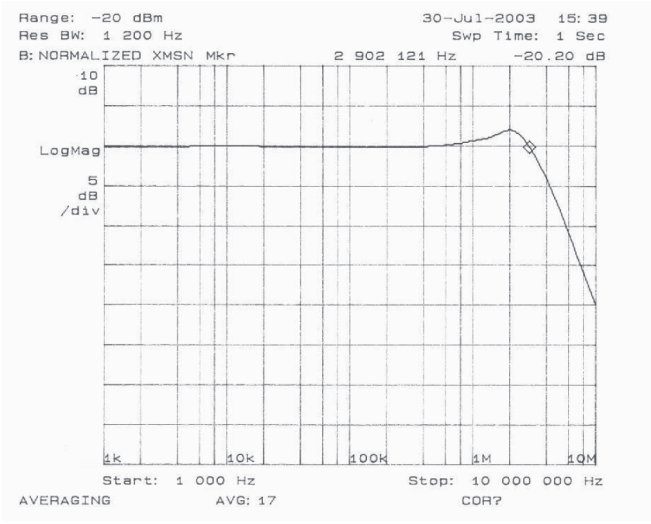

Fig. 6: Experimental AC response of CCII [6].

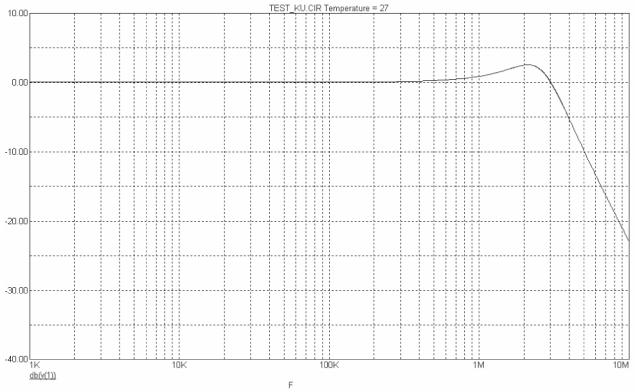

Fig. 7: AC response of proposed macromodel.

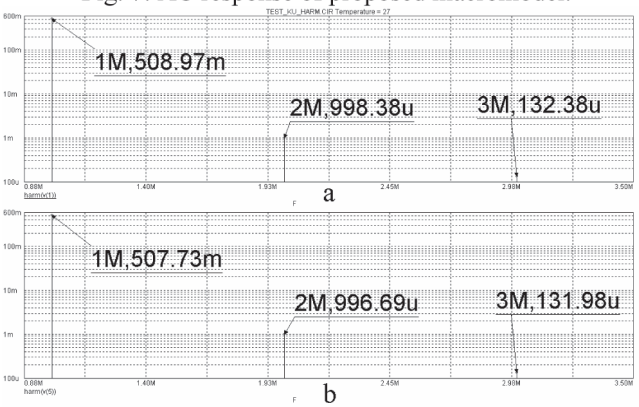

Fig. 8 The results of simulation of harmonic distortions (a – transistor-level CCII, b – proposed macromodel).

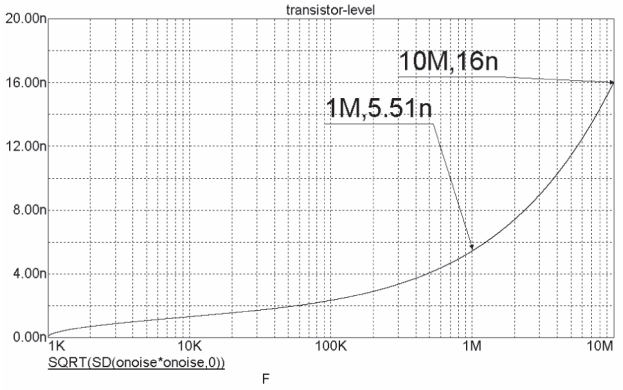

Fig. 9: RMS noise current at *Z*-terminal for transistor-level CCII.

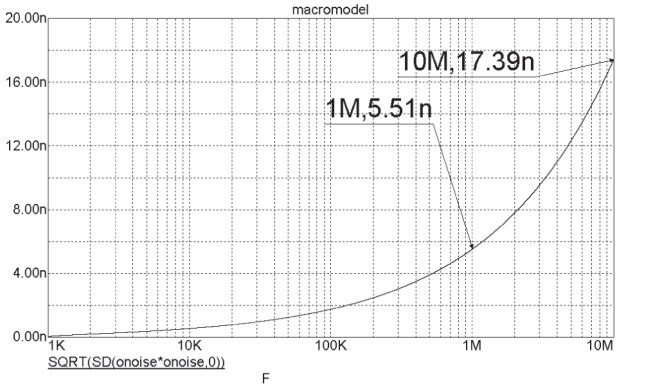

Fig. 10: RMS noise current at *Z*-terminal for proposed macromodel of CCII.

Results of transistor-level and macromodel simulations are shown in Fig. 8.

Finally, results of noise analyses for transistor-level CCII and macromodel are shown in Fig. 9. The simulation was performed when terminals *Y* and *Z* had been grounded and noise current at *Z*-terminal was determined by means of current controlled voltage source to convert current noise to voltage noise.

VI. Conclusion

The macromodel of CMOS second generation current conveyor has been proposed. Frequency, nonlinear, and noise properties have been taken into account in the model. Results of computer simulations and the comparison with experimental data and with transistor-level simulation demonstrated an accuracy of the approach.

REFERENCES

[1] A.Korotkov, D.Morozov, A.Tutyshkin, H.Hauer, R.Unbehauen, "Design of a CMOS high frequency current conveyor based switched-capacitor filter with low power consumption," In Proc. MWCAS'2003, Cairo, Egypt, 2003.

[2] N.Tarim, B.Yenen, H.Kuntman, "Simple and accurate non-linear current conveyor macromodel suitable for simulation of active filters using CCIIs," Int. J. Circuit Theory and Applications, vol.26, no.1, pp.27-38, 1998.

[3] N.Tarim, B.Yenen, H.Kuntman, "Simple and accurate nonlinear current conveyor macromodel," In Proc. MELECON'96, Bari, Italy, vol.1, pp. 447-450, 1996.

[4] E.Bruun, "Noise properties of CMOS current conveyors," In Proc. ISCAS'96, Atlanta, vol.I, pp. 144-147, 1996.

[5] E.Bruun, "Analysis of the noise characteristics of CMOS current conveyors," Analog Integrated Circuits and Signal Processing, vol.12, pp.71-78, Jan. 1997.

[6] C.Toumazou, F.J.Lidgey, D.G. Haigh, Analogue IC design: the current-mode approach, Peter Peregrinus Ltd., IEE Press, London, 1990.