IMPLEMENTATION OF FPGA-BASED DVB-T2 TRANSMITTER FOR A SECOND GENERATION DIGITAL TERRESTRIAL TELEVISION BROADCASTING SYSTEM

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ABSTRACT

Nowadays, with strong development of Science and Technology, integrated circuits continue to dominate not only in the field of digital information. Over the last several years, Technological television industry has taken huge strides and powerful transformation to meet with government's policy about digitization of television all over the country in period 2015 - 2020. Stemming from the practical needs of "localization of products" and mastering of technological design of DVB-T2 transmitter (Digital Video Broadcasting - Terrestrial for Second generation), the authors have made an effort to research in algorithm, designed and tested in Field Programmable Gate Array (FPGA) technology. DVB-T2 is mainly aimed to replace the current standard DVB-T. The main motivation of DVB-T2 is to provide broadcasters with more advanced and efficient alternative to DVB-T standards. In DVB-T2 transmitter system, digital audio, video, and other data are compressed into a single signal to be transmitted on a single RF channel, using orthogonal frequency-division multiplexing (OFDM) with concatenated channel coding and interleaving. The higher offered bit rate makes it a suited system for carrying HDTV signals on the terrestrial TV channel. The next generation broadcasting systems should be designed to make full use of spectral resources while providing reliable transmissions in order to enable services like multichannel HDTV (High Definition Television) and innovative data casting services. The efficient usage of the radio spectrum can be achieved by the introduction of Single Frequency Networks (SFN). Digital transmitter DVB-T2 implemented on FPGA using a software Xilinx System Generator for DSP tool and Xilinx ISE Design Suite 14.7. System Generator for DSP is in conjunction on environment MATLAB-Simulink that is capable of simulating the proposed hardware structures that is synthesized and implemented by the programmable elements in Field-programmable Gate Arrays. In this project, adaptative MPEG-TS bitrate converter is designed to allows to increasing or reducing the MPEG TS rate by adding or filtering NULL packets. The entire digital transmitter DVB-T2 is integrated in one chip Xilinx FPGA Kintex-7 XC7K325T-1FFG676. Experimental design on development Kit NetFPGA-1G-CML of Digilent Corporation is performed at design department of technology center of Vietnamese Communications Television Development JSC. Authors are continuing to improve products, put into practical applications to replace the digital terrestrial television broadcasting stations that are being used in Vietnam. The article named "Implementation of FPGA-based DVB-T2 transmitter for a second generation digital terrestrial television broadcasting system" presents the research results, design methods, test results to compare, evaluate the accuracy of algorithm implementation. The results open up new directions for technological television in Vietnam.

KEYWORDS: *cardiovascular diseases, random forest, k-neares*

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The article presents the main results obtained in Vietnamese OJSC "Development of communication-television", on the implementation of second-generation terrestrial digital television system transmitter (European standard DVB-T2 on FPGA).

The block diagram is shown in Figure 1.

The input processing module (MBO) is considered in the mode of a single-stream (in mode 'A' [1, 8-10]) physical layer channel (PLP). MBO assembles data from an MPEG-TS transport stream into groups called streaming (Baseband) frames (BB frames) according to modulation and coding parameters. As in the conference report [2], a specific implementation of MBO on FPGA with optimization of resources and processing speed is presented. Parameters for DVB-T2 system can be selected in [3]. In MBO (Figure 2 [1]) two parts are included: mode adaptation (ingress interface, convolutional CRC-8 coding, BB header addition) and stream adaptation (padding insert, BB frame scrambling).

To achieve the desired bit rate from the MPEG generator, the MPEG signal is fed over the coaxial cable to the Bitrate adapter [4].

During the design phase, pseudo-random data generated in the FPGA chip is received to evaluate each block of the system. The generator polynomial and the diagram (Fig. 2) for generating the MPEG data stream is proposed in Fig. 2 [5].

Diagram of DVB-T2 system on FPGA, including control points, is shown in Figure 3 [5].

Post-MBO data stream will be protected by Bose-Chowdhury-Hawkingham Error Correction (BCH) coding and Low Density Parity Check (LDPC) coding. Processing of data streams by MBO module and a combination of BCH and LDPC coding meets the requirements of the DVB-S2 satellite digital television system. With its strong error correction capability, combining BCH and LDPC, the DVB-T2 system achieves high power over DVB-T by 50% in multi-frequency networks. In addition, the constellation rotation in DVB-T2 has the ability to receive a signal with a large coding ratio.

BCH correcting coding (*Nbch, Kbch*) must be applied to every BBFRAME frame to form an error-proof packet. Where, *Kbch* is the length of the BBFRAME of the frame that enters the BCH code, Nbch is the length of the data block, including the BBFRAME frame and the BCH data behind it. *Kldpc* = *Nbch* is the length of the data block that is received in the LDPC code. Nldpc is the length of the data at the output of the LDPC code. Parameters *Nbch, Kbch* are selected in table 6a/6b [1]. The generator BCH polynomial of the encoder to correct *t* errors is obtained by multiplying the first t polynomials in table 7a/7b [1].

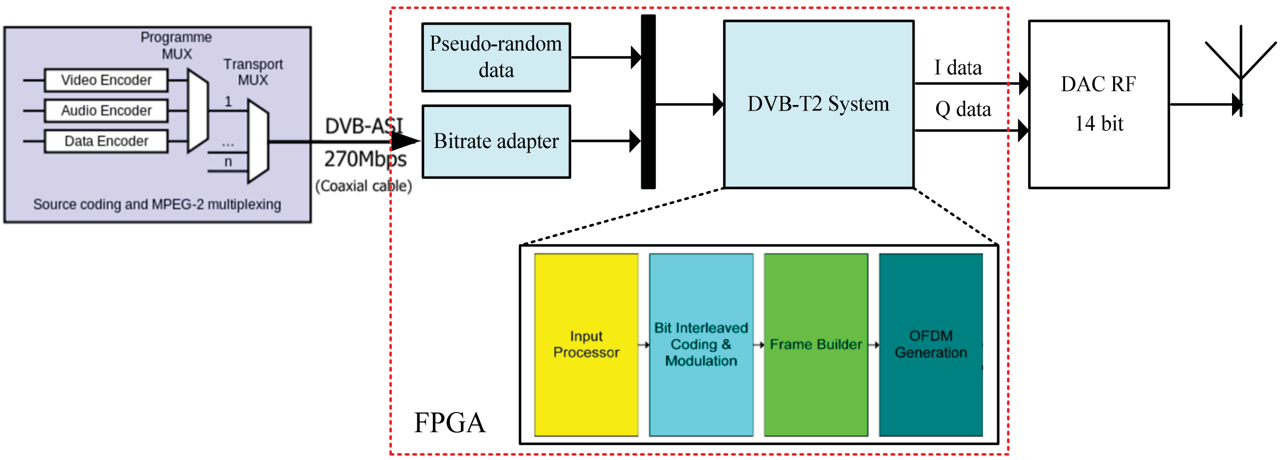

Figure 1

Таблица 1

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	53,466	407,600	13%
Number of Slice LUTs	91,689	203,800	44%
Number of occupied Slices	29,777	50,950	58%
Number of RAMB36E1/FIFO36E1s	302	445	67%
Number of RAMB18E1/FIFO18E1s	60	890	6%
Number of DSP48E1s	72	840	8%

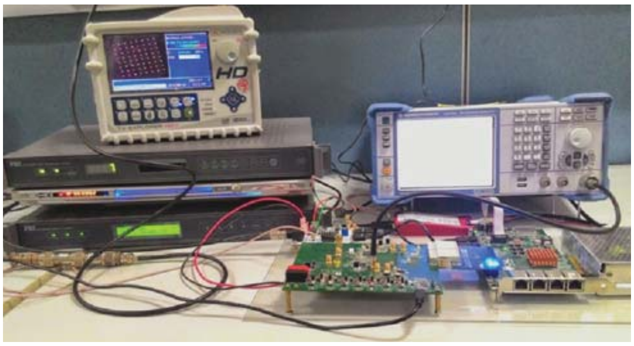

Figure 2

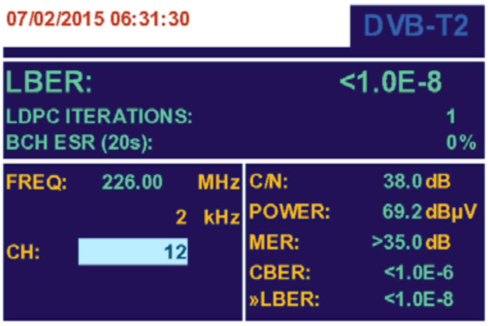

Figure 3

A code with a low density of parity checks is a code used in information transmission, a special case of a block linear code with a parity check. Special feature is low density of check matrix significant elements, due to which the relative simplicity of coding tools implementation is achieved, containing mainly zeros and a relatively small number of ones. Positions of the units are shown in Appendix A and B [1].

After the bit interleaver, the data is modulated.

The framing unit implements the mapping of data cells after modulation and rotation of the constellation and signaling into subcarriers. To improve the spectral characteristics of signal, subcarriers are frequency interleaved.

The OFDM shaping module uses a large number of closely spaced orthogonal subcarriers. Each subcarrier is modulated in a conventional modulation scheme at a low symbol rate, maintaining the overall data rate as conventional single carrier modulation schemes in the same bandwidth. In practice, OFDM signals are obtained by using an FFT (Fast Fourier Transform).

As a result of the inverse fast Fourier transform (IFFT) of N carriers, a pulse signal is generated for the value of difference between the maximum peak value and target power value. Therefore, PAPR method is designed to reduce peak-to-average power ratio.

Each block and module is separately implemented on FPGA. The results of processing from control points are compared with reference dataset [6].

DVB-T2 system is implemented on Xilinx Kintex-7 XC7K325T-1FFG676 chip of Digilent NetFPGA-1G-CML Development Kit [7]. The entire system is integrated on a single chip with resources shown in Table 1.

The results are shown in Figures 2-3.

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