# EFFICIENT IMPLEMENTATION OF FPGA-BASED FORWARD ERROR CORRECTING COMBINATION AND BIT TO CELL WORD DE-MULTIPLEXER FOR A SECOND GENERATION DIGITAL TERRESTRIAL TELEVISION BROADCASTING SYSTEM

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**ABSTRACT**

This report focus on the implementation of FEC part. The motivation of the design is that FEC is an effective tool to mitigate problems associated with OFDM which stem from multipath fading channel, high speed data rate. One of the key features of BCH codes is that during code design, there is a precise control over the number of symbol errors that are correctable by the code. BCH coder proccesses parralelly with high-speed operation. 8-bit parallel data input and output helps to maximize the through-put. DVB-T2 used LDPC coder, as inner codes with word length up to 64,800 bits, enabling significant proximity to Shannon limit. This encoder supports all code rates and both normal and short frames. Output of LDPC encoder is interleaved with bit interleaver.

This project was fully optimized for speed and memory area, fully synchronized by using a single clock. The design was coded in VHDL, synthesized by using Xilinx ISE Design Suite 14.7. The design has been tested on development Kit NetFPGA-1G-CML of Digilent Corporation and the bit map was downloaded into Xilinx Kintex-7 XC7K325T-1FFG676, which is integrated on experimental transmitter system DVB-T2. This research product belong to program "Research of experimental testing of second generation digital terrestrial television broadcasting system DVB-T2" of Vietnamese Communications Television Development JSC.

**KEYWORDS:** *cardiovascular diseases, random forest, k-neares*

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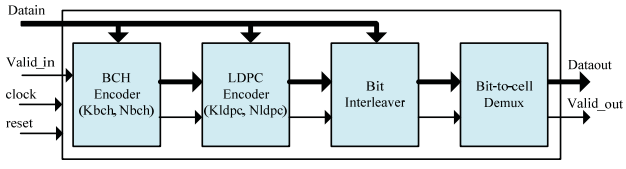
DVB-T2 (Digital Video Broadcasting - Terrestrial for Second generation) is a transceiver system of modern digital television nowadays, which have strong resistance to interference due to concatenated channel coding and bit interleaving combination. The forward error-correcting (FEC) includes Bose-Chaudhuri-Hocquenghem multiple error correction binary block code (BCH), Low Density Parity Check coder (LDPC) and bit interleaver. This coding combination has been developed by Xilins into IP Core based on the standard that used for DVB-S2 system and can be used compatibly for system DVB-T2.

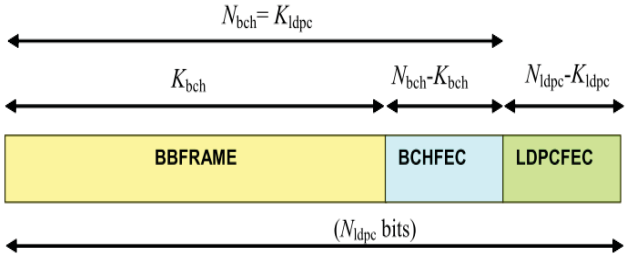
However, as well as other commercial companies in the world, product IP Core is copyrighted, users have to purchase the license and that license is used only one time for one computer. Morever, the final version LogiCORE IP DVB-S.2 FEC Encoder v2.0 of the Xilinx from 02/12/2009 has not developed further and integrated into programming Xillinx tools of FPGA. Therefore, the article named “Efficient implementation of FPGA-based forward error correcting combination and Bit to cell word de-multiplexer for a second generation digital terrestrial television broadcasting system” presents the design of a single FPGA intellectual property (IP) core for channel coding combination and Bit to cell word de-multiplexer. This design will be an open source for products of digital television systems.

This report focus on the implementation of FEC part. The motivation of the design is that FEC is an effective tool to mitigate problems associated with OFDM which stem from multipath fading channel, high speed data rate. One of the key features of BCH codes is that during code design, there is a precise control over the number of symbol errors that are correctable by the code. BCH coder proccesses parralelly with high-speed operation. 8-bit parallel data input and output helps to maximize the throughput. DVB-T2 used LDPC coder, as inner codes with word length up to 64,800 bits, enabling significant proximity to Shannon limit. This encoder supports all code rates and both normal and short frames. Output of LDPC encoder is interleaved with bit interleaver.

According to the literature [1, 8-10], the MPEG data stream after the input processing module is protected by a combination of BCH and LDPC. Then the bits are interleaved and modulated. The structural design diagram is presented below:




In general, this scheme is based on the Xilinx IP core, as shown in Fig. 1 [2]. The difference with Xilinx IP Core is that our design does not use a FIFO, but rather takes memory to store and process data. Therefore, the memory size is small. The data frame format is depicted in the following figure.




Where, $K_{bch}$ - the length of the BBFRAME of the frame supplied to the BCH code, Nbch is the length of the data block, including the BBFRAME frame and the BCH data behind it.$K_{ldpc} = N_{bch}$ - this is the length of the data block that is received in the LDPC code. $N_{ldpc}$ - data length at the LDPC code output.

As in [3], a specific implementation of BCH on FPGA with optimization of resources and processing speed is presented. The parameters of the BCH and LDPC codes Nbch, Kbch are selected in table 6a for the data stream, and for signaling in table 6b [1]. BCH correcting coding (Nbch, Kbch) must be applied to every BBFRAME frame to form an error-proof packet. The BCH generator polynomial of the encoder to correct t errors is obtained by multiplying the first t polynomials in Table 7a / 7b [1].

$$g_1(x) \quad 1 + x^2 + x^3 + x^5 + x^{16} \tag{1}$$

$$g_2(x) \quad 1 + x + x^4 + x^5 + x^6 + x^8 + x^{16} \tag{2}$$

$$g_3(x) \quad 1 + x^2 + x^3 + x^4 + x^5 + x^7 + x^8 + x^9 + x^{10} + x^{11} + x^{16} \tag{3}$$

$$g_4(x) \quad 1 + x^2 + x^4 + x^6 + x^9 + x^{11} + x^{12} + x^{14} + x^{16} \tag{4}$$

$$g_5(x) \quad 1 + x + x^2 + x^3 + x^5 + x^8 + x^9 + x^{10} + x^{11} + x^{12} + x^{16} \tag{5}$$

$$g_6(x) \quad 1 + x^2 + x^4 + x^5 + x^7 + x^8 + x^9 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15} + x^{16} \tag{6}$$

$$g_7(x) \quad 1 + x^2 + x^5 + x^6 + x^8 + x^9 + x1^0 + x^{11} + x^{13} + x^{15} + x^{16} \tag{7}$$

$$g_8(x) \quad 1 + x + x^2 + x^5 + x^6 + x^8 + x^9 + x^{12} + x^{13} + x^{14} + x^{16} \tag{8}$$

$$g_9(x) \quad 1 + x^5 + x^7 + x^9 + x^{10} + x^{11} + x^{16} \tag{9}$$

$$g_{10}(x) \quad 1 + x + x^2 + x^5 + x^7 + x^8 + x^{10} + x^{12} + x^{13} + x^{14} + x^{16} \tag{10}$$

$$g_{11}(x) \quad 1 + x^2 + x^3 + x^5 + x^9 + x^{11} + x^{12} + x^{13} + x^{16} \tag{11}$$

$$g_{12}(x) \quad 1 + x + x^5 + x^6 + x^7 + x^9 + x^{11} + x^{12} + x^{16} \tag{12}$$

Insert Kbch bits of the message arriving in the BCH code, M = (mKbch-1, mKbch-2, ..., m1, m0). First, we multiply the information word by xNbch-Kbch. We get:

$$(m_{Kbch-1}x^{Kbch-1} + m_{Kbch-2}x^{Kbch-2} + ... + +m_1x + m_0).x^{Nbch-Kbch} \quad (13)$$

где:

$$m(x) = (m_{Kbch-1}x^{Kbch-1} + m_{Kbch-2}x^{Kbch-2} + ... + + m_1x + m_0) \quad (14)$$

is called the message polynomial.

This multiplication is done in the FPGA chip by left-shifting (Nbch - Kbch) bits.

Then the resulting polynomial is divided by the generator polynomial g (x). The remainder will be:

$$d(x) = d_{Nbch-Kbch-1}\, x^{Nbch-Kbch-1} + ... + +d_1x + d_0 \quad (15)$$

Compilation of the output codeword I, which forms an information word for LDPC coding, namely:

$$I = (i_0, i_1, ...,i_{Nbch-1}) = (m_{Kbch-1}, m_{Kbch-2},..., m_1, m_0, d_{Nbch-Kbch-1}, ... d_1, d_0)$$

The equivalent polynomial of the codeword is

$$c(x) = m(x).\, x^{Nbch-Kbch} + d(x) \quad (17)$$

This is an *I* encoding word with length $K_{ldpc} = N_{bch}$ protected by LDPC code. He will calculate ($N_{ldpc}$ - $K_{ldpc}$) parity bit ($p_0$, $p_1$, ..., $p_{Nldpc\ -\ Kldpc-1}$) for each information block $k_{ldpc}$ bit ($i_0$, $i_1$, ..., $i_{Kldpc-1}$). As a result, we get the coding word Λ with length $N_{ldpc}$:

$$\Lambda = (\lambda_0, \lambda_1,...,\lambda_{Nldpc-1}) = = (i_0, i_1,...,i_{Kldpc-1}, p_0, p_1,...,p_{Nldpc-1}) \quad (18)$$

LDPC is a binary line parity code. A special feature is the low density of significant elements of the check matrix, due to which the relative ease of implementation of the coding tools is achieved. LDPC codes are described by a low density parity check matrix containing mostly zeros and a relatively small number of ones. The positions of the units are given in Appendix A and B [1].

The output data Λ of the LDPC encoder shall be bit interleaved, which consists of parity bit interleaving followed by a spin-column interleaving procedure. The output of the parity interleaver is U and the output of the spinning interleaver is V.

In the parity bit interleaver, the parity bits are interleaved according to the formulas:

$$u_i = \lambda_i \text{ , для } 0 \le i < K_{ldpc} \quad (19)$$

$$u_{Kldpc + 360t + s} = \lambda_{Kldpc + s.Qldpc + t} \text{ , для } 0 \le s < 360,\ 0 \le t < Q_{ldpc} \quad (20)$$

where $Q_{ldpc}$ specified in tables 8a and 8b [1].

In a spin-column interleaver, the data bits ui from the parity bit interleaver are alternately written column-by-column to the column-spin interleaver and are alternately read line-by-line therefrom. Input bit $u_i$ with index *i*, where $0 \le i < N_{ldpc}$, written to a column $c_i$, string $r_i$ interleaver, where:

$$c_i = i \text{ div } N_r \quad (21)$$

$$r_i = (i + t_{ci}) \bmod N_r \quad (22)$$

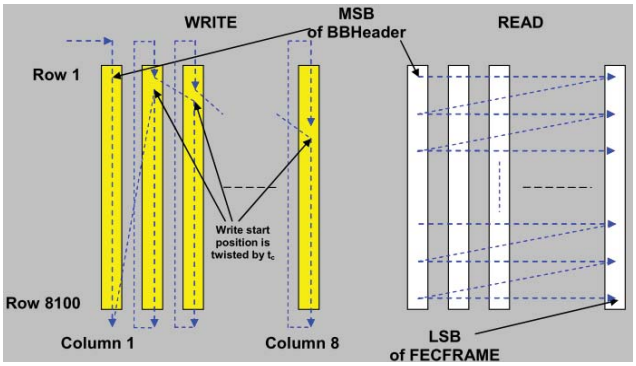
Input bit $v_j$ with index $0 \le j < N_{ldpc}$ read from string $r_j$, column $c_j$, where

$$c_j = j \text{ div } N_c \quad (23)$$

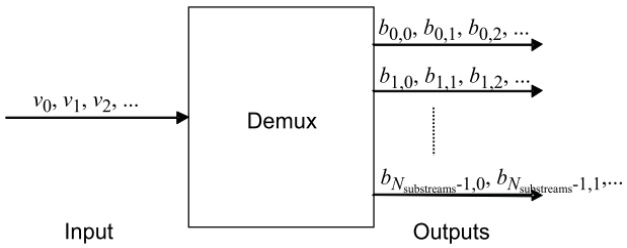
$$r_j = j \bmod N_c \quad (24)$$

where, $N_r$ и $N_c$ – the number of row and column of the bit interleaver, which depends on the type of modulation; the starting position of the record in each column is shifted by $t_c$ according to the table.

Bit interleaving scheme for standard FECFRAME frame length and 16-QAM.




After FEC encoding, the data is bit-demultiplexed into Nsubstreams of cell substreams to convert them to constellations. The number of Nsubstreams depends on the type of modulation and is indicated in table 12 [1], as shown in the following figure:




A set of design parameters is selected in [4]. The results obtained from control points 5, 6, 7a, 7 [5] are compared with the reference dataset [6].

The design is implemented on the Xilinx Kintex-7 XC7K325T-1FFG676 chip of the Digilent NetFPGA-1G-CML Development Kit [7]. The generated FPGA chip resource report for coding ratio 3/4 and modulation 64-QAM is shown in the following table.

Table

| Slice Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Registers | 34,203 | 407,600 | 8% |
| Number of Slice LUTs | 29,943 | 203,800 | 14% |
| Number of occupied Slices | 12,604 | 50,950 | 24% |
| Number of RAMB36E1/FIFO36E1s | 0 | 445 | 0% |
| Number of RAMB18E1/FIFO18E1s | 11 | 890 | 1% |
| Number of DSP48E1s | 0 | 840 | 0% |

This design was part of the project "Publishing the transmitter of the DVB-T2 system of the Vietnamese Television Development Company". The system is precisely functioning. Especially, the design is implemented in an open manner and has the ability to match with other television systems.

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