IMPLEMENTATION OF A REDUCED COMPLEXITY HIGH PERFORMANCE DATA ACQUISITION CHIP USING 0.18 MICRON TECHNOLOGY

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ABSTRACT

Data acquisition (DAQ) in the general sense is the process of collecting information from the real world. For engineers and scientists, this data is mostly numerical and is usually collected, stored and analysed using computers. However, most of the input signals cannot be read directly by digital computers. Because they are generally analog signals distinguished by continuous values, while computers can only recognise digital signals containing only the on/off levels. DAQ systems are therefore inevitably necessary, as they include the translation requirements from analog signals to digital data. For this reason, they have become significant in wide range of applications in modern science and technology [1]. The paper precents the disign of a 12-bit high-speed low-power Data Acquisition (DAQ) Chip. In this paper, the disigns of the building block components are aimed at high-accuracy along with high-speed and low power dissipation. A modifided flash Analog-to-Digital converter (ADC) was used instead of the traditional flash proposed DAQ chip operates at 1 GHz master clock frequency and achieves a sampling speed of 125 MS/s. It dissipates only 64.9 mW of power as compared to 97.2 mW when traditional flash ADC was used.

KEYWORDS: *Data acquisition, High-speed integrated circuits, Integrated circuit design, Analog-to-Digital Converter.*

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I. Introduction

Existing DAQ systems tended to use reasonably fast and accurate ADC, such as SA ADC. These systems can run at maximum 50MHz, providing the maximum data sampling rate of 150kS/s [2, 3]. They were the perfect solution for accuracy applications such as process control and test/measurement applications. However, applications such as high-end video signal processing, high performance wireless communication and power fault analysis [4, 5] require the signal sampling rate approaching 80MS/s. The existing DAQ systems, therefore, cannot fulfil this speed requirement. Out of all conventional ADCs, only flash ADC could provide the sampling speed beyond 100MS/s. However, flash ADC suffers from the main disadvantages of very large die size and high power consumption.

This leads to the need of architectures and circuit techniques enabling DAQ system to attain enhanced performance with reasonable chip area and power dissipation. In this DAQ design, emphasis was put on the reduction of system complexity and power dissipation while achieving a high sampling speed to satisfy current application requirements. The layout of the designed DAQ chip has also been implemented. The results of layout simulation have been back annotated, analysed and presented in this paper.

II. Da Acquisition Design

The typical building blocks of a DAQ system include an analog multiplexer (MUX), Programmable Gain Amplifier (PGA), anti-aliasing filter, Sample-and-Hold circuit (SHC), Analog-to-Digital converter (ADC) and a system controller, as shown in Fig. 1 where the ADC is the key element in the DAQ device.

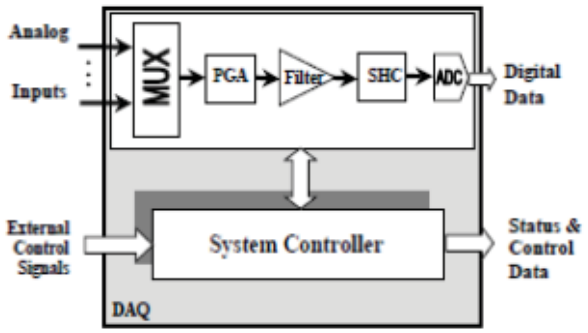

Fig. 1. Block Diagram of a Typical DAQ Chip

3.1. Analog Multiplexer

An analog MUX is one of the most sensitive parts of the design. It is the most responsible device for accurate sampling of multi-input channels. A MUX typically comprises of several switches connecting all of the input channels to the output end of the MU CMOS transmission gate (TG) is typically chosen to implement the switches due to its superior characteristics including high dynamic analog range and clock feedthrough error elimination. For the proposed DAQ system, a 4:1 analog MUX was designed allowing 4 channels to be processed. The binary control word (sel1sel2) selects the input using the following logic expression:

$$v_{out} = v_{in1}(\overline{sel_1}.\overline{sel_2}) + v_{in2}(\overline{sel_1}.sel_2) + v_{in3}(sel_1.\overline{sel_2}) + v_{in4}(sel_1.sel_2) \quad (1)$$

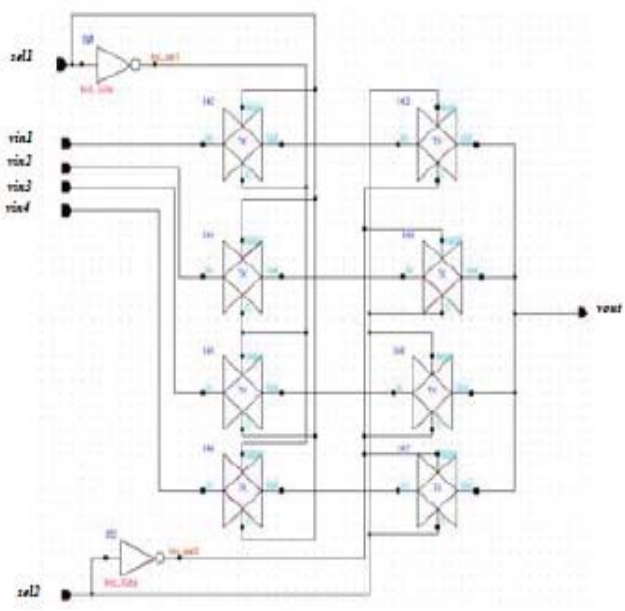

Fig. 2. Schematic diagram of 4:1 M1 MUX

3.2. Programmable Gain Amplifier

It is critical to have a PGA in a DAQ system to boost low-level input signals to maintain the linearity over the entire ADC bandwidth.

Figure 3 presents a PGA using feedback network to achieve high linearity. A current-mode amplifier with fixed equivalent feedback resistances of R_2 can maintain a constant feedback factor, regardless of the input equivalent resistances of R_1. Thus, the amplifier can be optimised for minimal power dissipation with a specific bandwidth [6]. With proper resistor design and transistor sizing, R_1 will be adjusted so that the average current signals in the resistors remain constant, leading to little change of linearity at the PGA's outputs.

Traditional Bipolar and BiCMOS continuous time transconductance filters usually trade off high linearity with increased noise. Similarly, conventional CMOS filters typically do not achieve a high dynamic range. CMOS switched capacitor (SC) filters achieve several advantages over its counterparts. It exhibits improved dynamic range, is more capable of handling large signals, and is capable of being programmable by changing its sampling frequency [7].

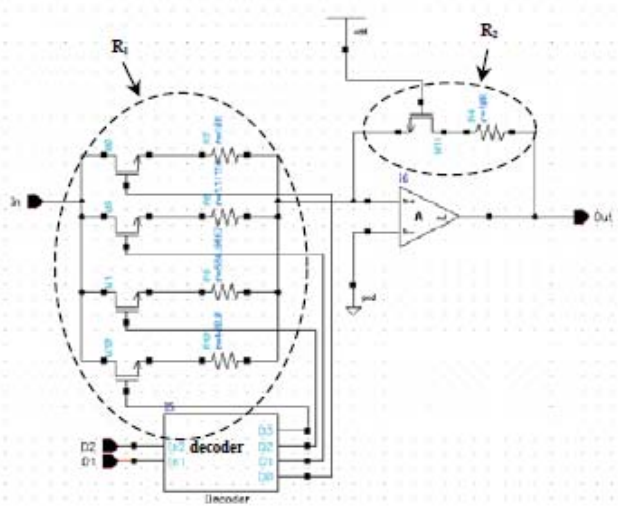

Fig. 3. Schematic Diagram of PGA

Fig. 4 illustrates a SC low pass filter comprising of an inverting integrator and a non-inverting integrator. The transfer function of the filter is described in equation (2). In the design, capacitors C4 and C5 compensate the offset voltage and DC gain error of the OPAM A1 and A2 respectively while capacitor C2 eliminates spikes (providing continuous feedback to the filter).

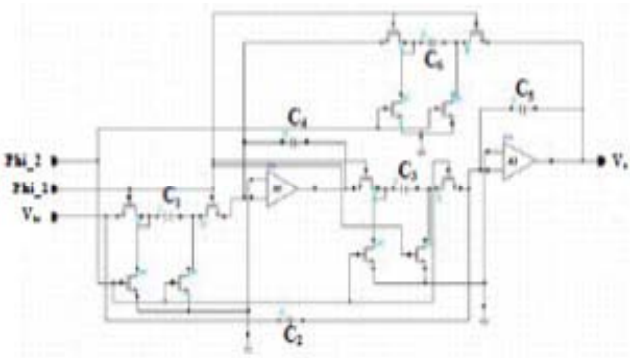

Fig. 4. Switched Capacitor Filter Schematic

$$H(s)=\frac{V_0}{V_i}=-\frac{C_4C_6+4\pi^2f^2f_c^2C_1C_3}{C_4C_5+4\pi^2f^2f_c^2C_2C_3} \qquad (2)$$

3.3. Sample-and-Hold Circuit

SHC is an important building block in DAQ system since the system throughput and accuracy are limited by the speed and precision at which the input is sampled and held.

Figure 5 depicts the schematic diagram of SHC architecture utilised in the proposed DAQ system.

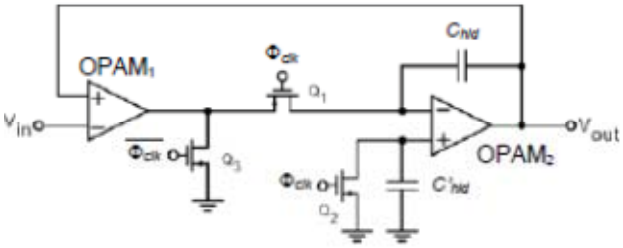

Fig. 5. SHC using feedback loop with compensate capacitor

In this circuit, the sampling switch Q1 is maintained at a virtual ground during the sampling phase and therefore the charge injection error is effectively removed. Also, a supplementary NMOS switch Q2, identical to Q1 and a compensate capacitor *C'hld*, identical to the holing capacitor *Chld* are added to eliminate the clock feedthrough error. This type of SHC, therefore, obtains a superior high-accuracy characteristic.

3.4. Analog-to-Digital Converter

Pipeline ADC consists of numerous consecutive stages, each stage containing a SHC, a low resolution ADC, Digital-to-Analog converter (DAC) and a summing circuit that includes an amplifier to provide gain [8], as shown in Fig. 6.

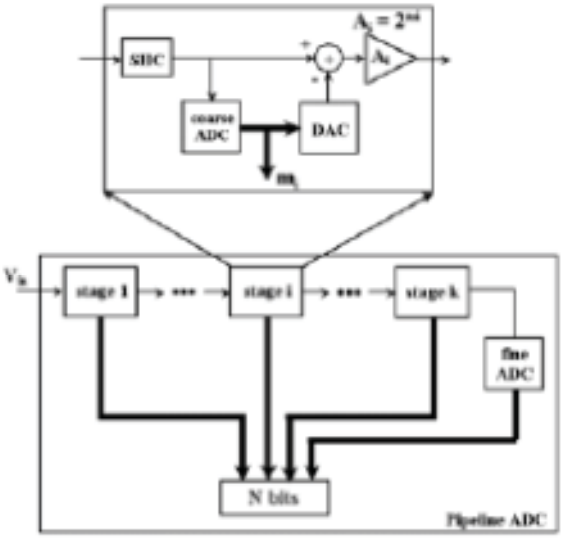

Fig. 6. Pipeline ADC Architecture

Flash ADCs are typically employed as coarse and fine ADCs in a pipeline ADC architecture. However, the major disadvantages of the full flash ADC architectures are high device power consumption, high device complexity and high device input capacitance.

A modified flash ADC [9, 10], as illustrated in Fig. 7, was used instead of the traditional full flash ADC to reduce design complexity and power dissipation.

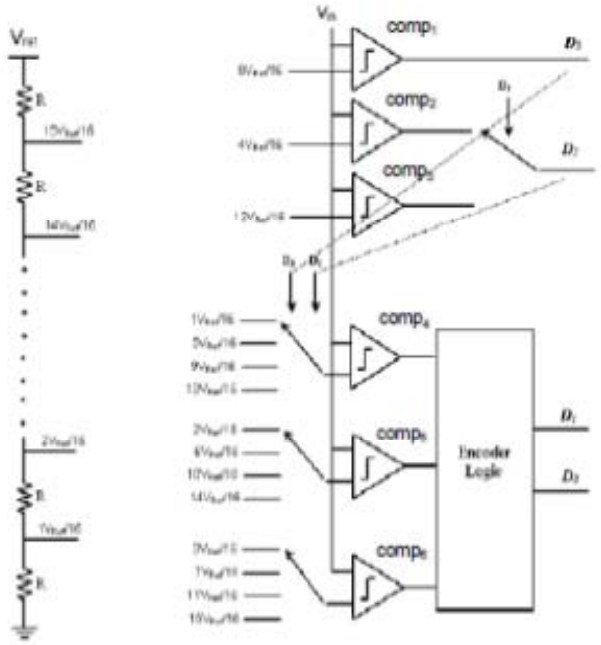

Fig. 7. Four-bit Modified Flash ADC

The modified flash ADC, which utilised an optimised latched-type comparator [11], can perform the Analog-to-Digital (A/D) conversion in one clock cycle (like a full flash ADC). The main advantage of the modified flash ADC approach is the great reduction in the number of comparators. Therefore the device obtains a great power saving and size reduction.

To obtain 12-bit resolution, the pipeline ADC is designed to have 3 stages, each stage contributes 4-bit resolution.

3.5. System Controller

The system controller should make logical decisions based on the input signals to instruct the constituent components (including 4:1 MUX, SHC and 12-bit 3-stage pipeline ADC) to perform their functions properly at the correct instance. Figure 8 shows the timing diagram of the constituent components that are directed by the system controller (time not to scale). The designed pipeline ADC includes 3 consecutive stages, thus the total pipeline ADC conversion time includes the conversion time of the three stages. Besides, the MUX channel selection can be performed before the start conversion because the SHC will keep the data until a next 'start' signal applied.

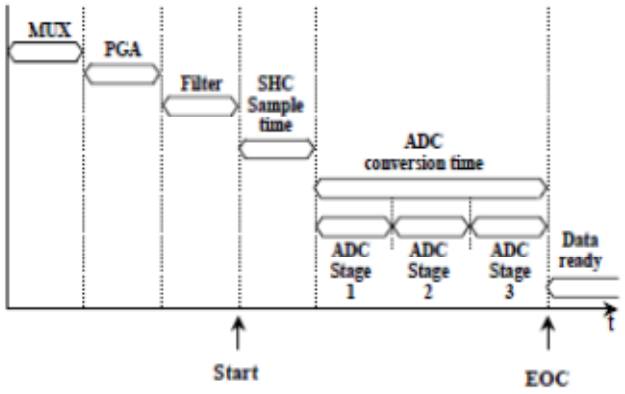

Fig. 8. DAQ system control signal timing diagram

III. sults

Two DAQ systems, using traditional 4-bit full flash ADC and the modified flash ADC topologies in a pipeline architecture, have been both implemented and simulated in Cadence. The performance of the two approaches are summarised in Table 1.

The layout of the designed DAQ chip employing the modified flash ADC to attain reduced power and complexity has been implemented and is illustrated in Fig. 9. The results of the layout simulation of the DAQ chip have been back annotated and analysed. Table 2 presents the simulation results of the layout DAQ chip.

IV. Conclus

A 12-bit, 4-channel fully CMOS DAQ chip has been presented. It operates at 1GHz master clock frequency and achieves a sampling speed of 125MS/s.

The DAQ system was implemented using both traditional flash ADC and modified flash ADC architectures. It can be seen that using the new modified flash approach greatly reduces the system power consumption. It dissipates only 64.9mW of power as compared to 97.2mW when traditional flash ADC was used.

Results indicate that a 33% power saving is obtained when the new modified flash ADC is used instead of a full flash ADC. This type of DAQ system is well suited for high-speed low-power applications, such as high performance wireless communication, where speed and power consumption are of main concern. It also benefits multi-channel applications, such as power fault analysis, where several channels can be assessed at high speed using only single PGA, anti-aliasing filter, SHC and ADC.

Table 1

Performance summary of the DAQ systems using traditional flash ADC and modified flash ADC

Device delay	Using traditional flash ADC	Using modified flash ADC
Total delay	8ns	8ns
Max data rate	125MS/s	125MS/s
Max master clock speed	1GHz	1GHz
Device power consumption @ 800MHz system master clock		
MUX power consumption	0.4mW	0.4mW
PGA power consumption	6.8mW	6.8mW
Filter power consumption	9.5mW	9.5mW
SHC power consumption	7.1mW	7.1mW
Pipeline ADC power consumption	72.9mW	40.6mW
Controller power consumption	0.5mW	0.5mW
Total Power consumption	97.2mW	64.9mW
Other Parameters		
DNL	±0.5 LSB	+0.6/-0.5 LSB
INL	±0.5 LSB	±0.5 LSB
Resolutions	12 bits	12 bits
Supply Voltage	2.5V	2.5V

Fig. 9. Layout implementation of the designed DAQ chip

Table 2

Simulation results of the layout DAQ chip

Description	12-bit DAQ chip (using modified flash ADC)
Power Consumption	77.1mW
Max master clock speed	917MHz
Area	3.52mm^2
Resolution	12 bits
Technology	0.18μm CMOS
Voltage Supply	2.5V

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