TIME-INTERLEAVED MIXED-SIGNAL TEST CORE DIGITIZERS

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DOI: 10.36724/2664-066X-2021-7-3-27-30

ABSTRACT

System-on-Chip (SoC) is one of the main driving forces that have been reshaping the consumer electronics industry. The SoC alternative to conventional systems design is growing in popularity as the device packing densi escalates due to the evolution of semiconductor technology. Moreover, the decrease in semiconductor feature size is permitting the increase of clock frequencies and component operating speed. These advancements necessitate the integration of system components due to package parasitics and lengthy interconnect. Furthermore, SoC devices offer a cheaper and more compact solution to the consumer electronics industry.An integrated mixed-signal test core approach to SoC data acquisition is a valued alternate solution to many of the problems involving conventional test. One such test core data conversion architecture incorporates a sub-sampling algorithm known as the multipass method of digitization. This method occupies a very small silicon area in exchange for an increased data conversion time. Time-interleaved test core digitizers provide the capability to reduce test time, increase sampling frequency and increase signal bandwidth. As an implicit result of this compact circuit and multipass processing methodology, significant reductions in noise and spurious tones are observed.

KEYWORDS: *mixed-signal, analog-to-digital, digitizer, time-interleaving, test*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

I. Introduction

The amalgamation of digital, analog, and mixed- signal components into a single integrated circuit (IC) presents test engineers with tremendous difficulties. The current mixed-signal automated test equipment (ATE) solutions involve off chip stimulus and measurement through SoC package pins or IC probes. The tradeoffs between test development time, device test time, ATE requirements and SoC design constraints (e.g. I/O pads) is one of the greatest challenges facing the test engineering paradigm.

The integrated mixed-signal test core [1] provides an alternative to conventional test of mixed-signal ICs. This work proposes that the test apparatus be integrated within the mixed-signal SoC. Test requirements of mixed-signal circuits are extremely diverse. As such, the test core incorporates an arbitrary waveform generator (AWG) for signal stimulus and a digitizer to capture analog results.

The test-core solution boasts many advantages. By integrating the test equipment many interconnect and packaging problems are resolved, the number of test I/O pins is reduced, and parallel testing is facilitated. Another advantage is that the characterization and production testing can be performed by the same test core. In short, the test core approach offers the ability to improve product time-to-market and reduce cost as the constraints on development and test time are relaxed and the ATE requirements are moderated.

In order to reduce costly silicon area, a very small, mostly digital, digitizer architecture was developed to implement within the test core. One of the most significant tradeoffs of this compact digitizer design is an increase in test time. The digitization algorithm, known as the multipass method [2], is responsible for the time-intensive capture of analog information.

Time-interleaved data conversion is an attractive method to increase the sampling frequency of ADCs. Time-interleaved ADC systems implement multiple ADCs each sampled at alternate instants of time. Hence, for every additional time-interleaved ADC the sampling frequency may be increased proportionally. Furthermore, each ADC is clocked at its specified operating speed maintaining the performance characteristics of the individual ADC.

The disadvantage of the multiple-ADC time- interleaved architectures is the mismatch errors between ADCs. Each ADC will produce different DC offsets, gain errors, distortion and clock skews resulting in an increased noise and possible spurious tones. However, research has demonstrated that these errors can be compensated or corrected for through concurrent or post-processing techniques [3, 4]. Other research proposes a randomization sampling technique to reduce spurious tones [5].

The integrated mixed-signal test core can greatly benefit from time-interleaving whereby increasing the sampling frequency can imply a reduction in test time. Moreover, the addition of digitizers to the test core solution results in the integration of additional comparators. Furthermore, the multipass method of digitization implicitly offers the capability to reduce noise and remove spurious tones resulting from comparator mismatch.

The test core was implemented in a 0.18-µm CMOS process. Test results confirm the advantages of time-interleaving test cores. An outline of the paper is as follows: Section 2 reviews the design and operation of the test core digitizer. The time-interleaved test core is described in Section 3. Simulation and experimental results are revealed in Sections 4 and 5, respectively. Finally, Section 6 summarizes the proposed test system.

II. Mixed-Signal Test Core Digitizers

The integrated mixed-signal test core digitizer uses the multipass method of analog-to-digital conversion. This method operates on the premise that a periodic waveform of a known frequency is to be digitized. The frequency of the input signal is set by the coherency principle such that $F_T = MFS/N$, where F_T is the input waveform frequency, F_S is the sampling frequency, N is the number of samples per input waveform period and M is the number of input waveform periods to be captured within a unit test period (UTP). A UTP is the time it takes to collect N samples of the input waveform (i.e. $UTP = M/F_T = N/F_S$). For coherency, M and N should be integers, and for maximum information gathering, they should also be relatively prime to one another.

The multipass system, illustrated in Fig. 1, uses a 1-bit quantizer to compare 2^D-1 DC reference levels to all points on the periodic input waveform, where D is the number of bits that the converter can resolve. For each input waveform pass (or UTP), one reference level is established and compared to all N points of the test signal. The test signal waveform is reconstructed by summing all the digital outputs from each UTP that correspond to the same sampled instant on the waveform.

For Example, Fig. 2 illustrates the test signal and DC reference for a complete digitization cycle when D=3, M=1 and N=16. Within each UTP the test signal is sampled 16 times and compared with a single reference level. The digital result from each sample is stored in memory. The output from a complete conversion may be conceptually rearranged, as shown in Fig. 2b, to reveal the test signal waveform.

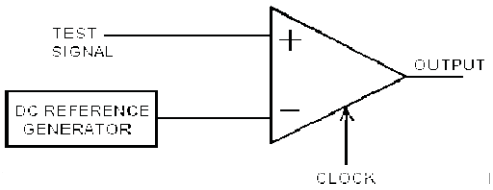
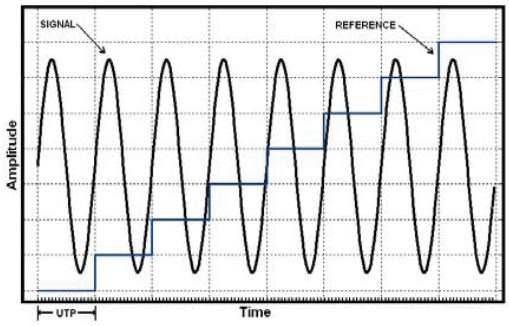
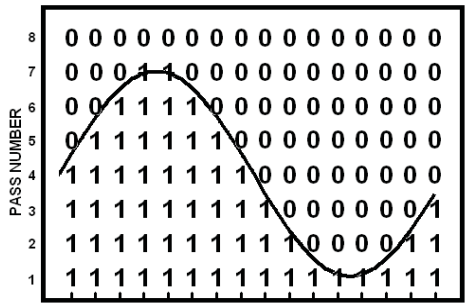


Fig. 1. Test Core Digitizer Architecture

The signal is reconstructed by summing the columns of Fig. 2b, as seen by the sinusoidal overlay. Alternatively, the output could be interpreted as a thermometer code.



(a)



(b

Fig. 2. 3-Bit Multipass Digitization Example (a) Input Test Signal and Reference; (b) Digital Recombination Process

At sampling clock periods smaller than the settling time of the comparator, a sub-sampling scheme would be employed within the multipass method, thus increasing the time to test. Time-interleaving multiple test core digitizers (i.e. comparators) can increase the effective sampling rate. By increasing the sampling frequency, sub-sampling would no longer be required.

III. Time-Interleaved Test Core Dig ers

The sampling frequency of an ADC is limited by circuit constraints and the tradeoffs between resolution and operating speed. Moreover, the input signal bandwidth of an ADC may be restricted by the maximum sampling frequency (i.e. Nyquist principle). Time-interleaved data conversion is an attractive method to increase the sampling frequency of ADCs. However, mismatch effects in these devices severely limit its performance by way of increased noise and spurious tones.

A time-interleaved mixed-signal test core system with five comparators is illustrated in Fig. 3. Each comparator will incorporate an input sample and hold stage and an output latch which are clocked by a phase generator. The comparators are stimulated by the same analog test signal and DC reference. Hence, the total design size only increases by the size of the additional four comparators. More importantly, the test time reduces by a factor of five.

IV. Simulation Resu

Using MATLAB the multipass method of digitization was simulated using the time-interleaved arrangement shown in Fig. 3.

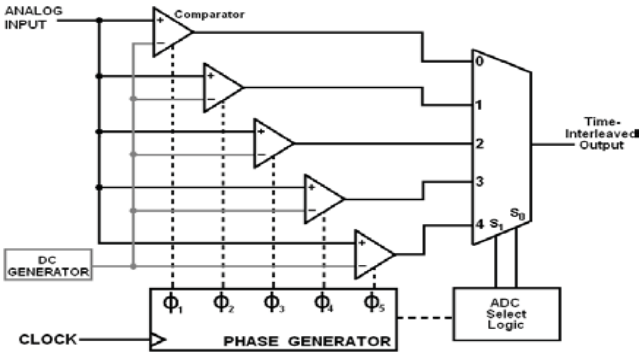
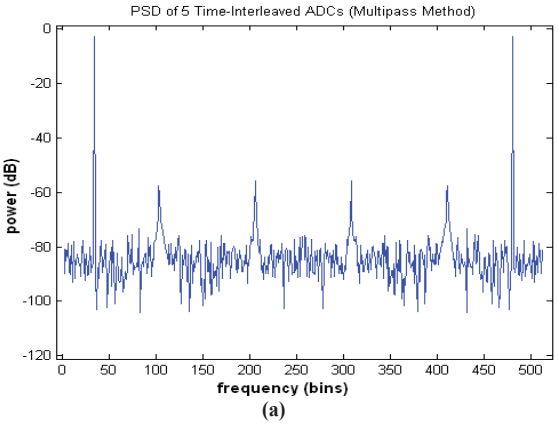


Fig. 3. Five Time-Interleaved Test Core Digitizers

Several sampling schemes were implemented to demonstrate the advantage of the test core.

The first sampling scenario, resulting in the power spectral density (PSD) shown in Fig. 4(a), involves reusing the same comparator to capture the same point in every pass of the multipass method. In this situation the mismatch between each comparator results in spurious tones. This situation is the typical result from any time-interleaved ADC system.



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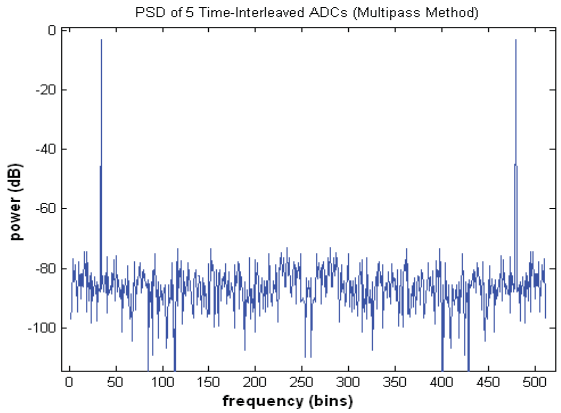


(b)

Fig. 4. Simulation Results Demonstrating the Multipass Benefit of Noise and Spurious Tone Suppression, (a) Time-Interleaved Digitization Mismatch Effects, (b) Multipass Method Suppressing Spurs

The second method of sampling consisted of rotating the comparators such that a different comparator, selected sequentially, is used to capture the same points in every pass.

Fig. 4(b) presents the PSD from this sampling method. It is clearly seen that the spurious tones are removed. In effect, the systematic mismatch errors have been evenly spread over the reconstructed waveform, thus contributing to the DC component. The distortion mismatch errors have been distributed over the entire signal bandwidth. The net difference between the two sampling conditions is a slightly better SNDR but a significantly improved SFDR. Most importantly, in conventional time-interleaved ADC systems, the second sampling algorithm is not possible.

V. Experimental Results

The time-interleaved test core digitizer, depicted in Fig. 3, was implemented in a 0.18-µm CMOS process. The microphotograph of the fabricated IC is shown in Fig. 5. The IC was tested using a Teradyne A567 ATE. Fig. 6(a) demonstrates the time-interleaved test core digitizer when each comparator is used to capture the same points through every pass of the multipass method. Fig. 6(b) results when alternating comparators are used to sample the same points from each pass.

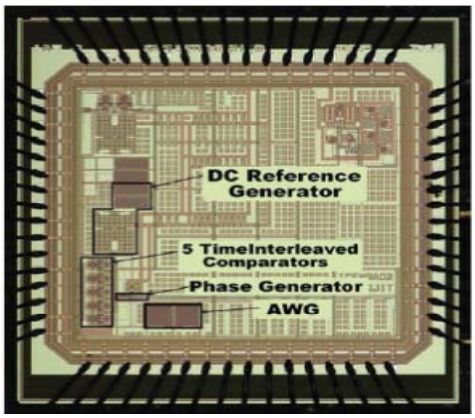


Fig. 5. Microphotograph of the Integrated Time- Interleaved Mixed-Signal Test Core in a 0.18-µm CMOS Process

Table 1 provides some of the numerical transition parameter results from each figure. It may be seen that SNR and SNDR are slightly better when the comparator usage is varied for each DC reference. However, the SFDR due to the mismatch induced spurs has increased 17 dB!

Table 1

Comparison of Figure 6 (a) and (b) Dynamic Performance Results

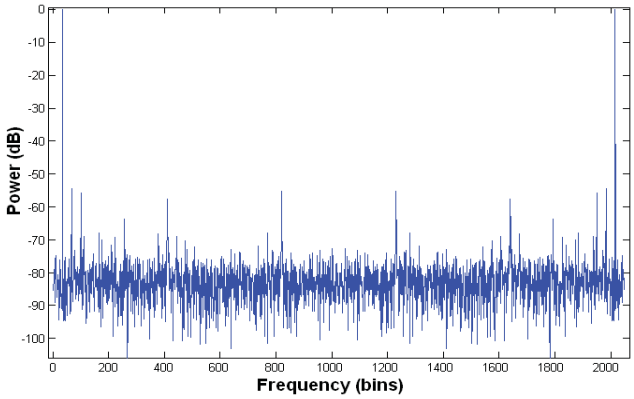
	Figure 6 (a)	Figure 6 (b)
SNR	48 dB	51 dB
SNDR	46 dB	48 dB
SFDR †	55 dB	72 dB

† comparing mismatch-induced spurs (not including harmonics)

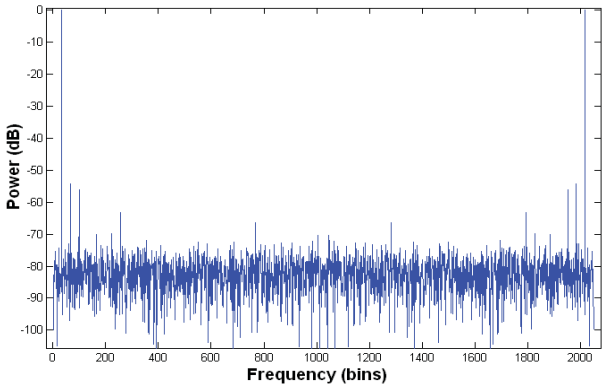
A second experiment was performed to demonstrate that there is no performance degradation between a single digitizer and the time-interleaved counterpart. While sampling a 160 kHz test signal at 10 MHz a single test core digitizer assumed a SNDR of 48 dB. The five time-interleaved test core digitizer achieved a SNDR of 49 dB.

VI. onclusion

The mixed-signal test core digitizer is an attractive alternative to conventional test of high performance SoCs. This area efficient design suffers a lengthier test data conversion time. Time-interleaving can reduce test time at an area cost of additional comparators. It was demonstrated that no performance degradation is observed due to comparator mismatch.



(a)



(b)

Fig. 6. Experimental Results Demonstrating the Multipass Benefit of Noise and Spurious Tone Suppression, (a) Time-Interleaved Digitization Mismatch Effects, (b) Multipass Method Suppressing Spurs

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