A 19 MW, 12.5 B, 2.1 MS/S SINGLE-BIT ΔΣ ADC IN 0.18 μm DIGITAL CMOS PROCESS

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ABSTRACT

The increasingly stringent requirements of today's communication systems and portable devices are imposing two challenges on the design of high-resolution, high-speed ADCs and delta-sigma modulators (ΔΣMs) in particular. The first is the extension of the input frequency range to include applications where the input bandwidth exceeds the 1 MHz range, while maintaining a feasible sampling frequency. The challenge in extending the operational speed of ΔΣMs is further rendered more complicated by the ever shrinking transistor dimension, and in turn, the supply voltage, hence the second challenge. To address those two challenges, the ΔΣMs presented in this paper targets a minimum of 12 bits in resolution at 2 MS/s Nyquist conversion rate, while using a single 1.8 V supply and minimum power dissipation.A switched-capacitor (SC) ΔΣ ADC integrated circuit (IC) with output rate slightly exceeding 2 MS/s was successfully implemented in a 1.8 V, 0.18 μm standard CMOS process. The IC consists of a fourth-order, multi-stage (2-1-1), single-bit modulator sampled at an oversampling rate of 50 MHz. Special effort has been made to reduce the power consumption of the modulator through careful system-level modeling and synthesis of circuit specifcations. Experimental results reveal a 77.6 dB dynamic range while consuming 18.8 mW of power, making it the lowest power dissipation for output rates in excess of 2 MS/s.

KEYWORDS: *digital CMOS process, portable devices, feasible sampling frequency.*

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1. Introduction

While many state-of-the-art lowpass ΔΣMs integrated circuits are published in the literature, some of which are presented in [1]-[5], they vary in their performance, output rate, power dissipation, technology, choice of architecture and sampling frequency, f_S. With this wide range of design criteria, it is unclear as to which modulator provides the best "overall" performance. While some modulators might have a superior resolution, the power dissipation could be very large too. It is therefore important that we make proper comparison using the most relevant metrics. It is those metrics discussed in Section 5, Modulator Comparison, that will reveal the superior performance of the experimental results of the circuit presented in this paper.

Following the introduction and the motivation behind this work, Section 2 of this paper presents a system-level description followed by the design of the main building blocks of the modulator in the third section. Experimental results demonstrating the functionality and performance of the ΔΣM are presented in Section 4, while performance comparison to other state-of-the-art modulators is presented in the Section 5. Concluding remarks are given in the last section of the paper.

2. SYSTEM-LEVEL DESIGN

In order to achieve good overall performance, it was important to minimize the power dissipation. In order to do so, the architecture had to be selected f rst. Then, it was essential to choose the minimum specif cations on each building block in the modulator that meet the target dynamic range. This was achieved through modeling the amplif er's bandwidth, slew rate, thermal noise, the comparator's offset, the input sampling network distortion and thermal noise contribution, all at the system-level. Once modeled, a set of design specif cations for the modulators's building blocks could be synthesized. With this modeling and synthesis, over-designing the modulators' building blocks is prevented which in turn keeps the power dissipation minimal. The details of the modeling and a new optimization and synthesis method that is computationally eff cient are presented elsewhere. Interested readers are referred to [6][7]. While the system-level design is one of the important keys in achieving a good resolution, the goal of this paper will be focused on the circuit implementation and the experimental results. The effectiveness of the synthesis method will be verif ed through the implementation of a fourth-order, cascade architecture consisting of three stages (2-1-1), all having single bit quantizers. With a minimum of 12 bits as a target resolution, an oversampling ratio, OSR, of24 is needed. With this OSR and an input bandwidth slightly exceeding 1 MHz, the corresponding sampling frequency, fs, is 50 MHz [5].

A summary of the non-idealities considered and their synthesized values are presented here and are shown in Table 1.

Table 1

Summary of synthesized versus implemented circuit specif cations

Block	Non-Ideality	Synthesized	Designed
OTA (C_L=1.5 pF)	DC Gain (dB)	72	100
	Gain-Bandwidth (MHz)	293	410
	Slew Rate (V/μs)	220	236/246
	Input Thermal Noise Density ($nV/\sqrt{Hz}$)	3.1	2.36
Comparator	Offset (mV)	60	-
Switch	$R_{max} = f(V_{in})$ (Ω)	540	119

3. SC CIRCUIT IMPLEMENTATION

The mapping of the previously synthesized block specif cations to a switched-capacitor implementation is presented in this section. In particular, the design of the operational transconductance amplif er (OTA) is presented in details followed by other blocks such as the comparator, the switches, the clock generator, the capacitors and the full circuit implementation.

3.1. OTA

A single-stage OTA was used due to its excellent frequency characteristics. A two-stage operational amplif er was avoided as it becomes power-hungry in low-voltage applications. The single-stage OTA was implemented using the folded-cascode topology with complementary differential pair at the input and n- and p as gain boosting stages at the output, as shown in Figure 1.

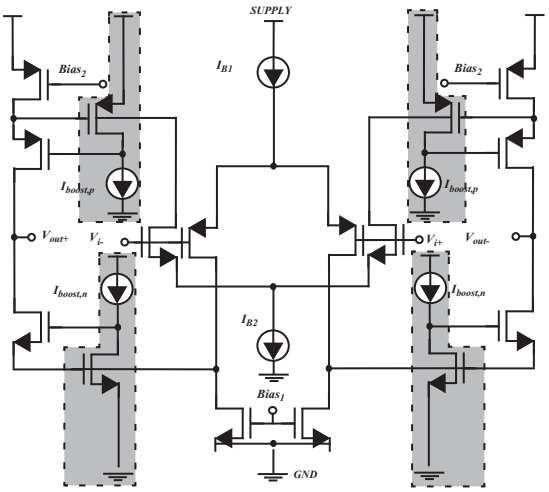

Fig. 1. OTA schematics with n- and p-gain boosting stages highlighted

The addition of the gain boosting results in an increase in the output impedance on the order of magnitude $g_m \cdot r_o$, which in turn results in an increased OTA DC gain.

On the other hand, the addition of the complementary differential pair at the input of the OTA has the advantages of increasing the bandwidth and providing a faster step response [8]. This is the result of increasing the effective transconductance, $g_{meffective}$, which becomes the sum of both transconductances g_{mdiff} and $g_{mdiffcomp}$.

As a result, the DC gain and bandwidth are increased by a factor equal to $(g_{mdiffcomp} + g_{mdiff})/g_{mdiff}$. The addition of the complementary differential pairs allows also for a larger OTA input swing.

The above advantages happen at the expense of increased power consumption and increased parasitic capacitances, and if not designed properly could result in excessive high frequency performance degradation where the single-stage OTA behaves more like a multi-stage design.

In order to optimize the sizing and biasing of the transistors, small-signal analysis was performed. In [8] and [9], the small-signal analysis was detailed for gain-boosted telescopic amplifiers, and was used here as a guideline with the appropriate modifications for the OTA topology under considerations. Detailed pole-zero map analysis was carried out in order to carefully size the biasing current and the transistors in the gain boosting stages and the complementary differential pairs to increase the OTA DC gain and bandwidth without degrading its frequency behavior. The effect of sizing both gain boosting stages (for given currents in the different branches of the OTA and given saturation voltages) was simulated in Matlab with transient and AC analysis performed. Corresponding pole-zero maps were also plotted to observe the locations of the poles and zeros as the current in the gain boosting stages was varied.

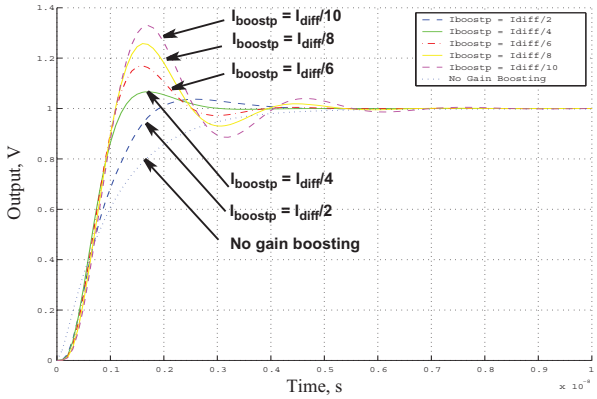

Fig. 2. Step response of the OTA as a function of the p-stage gain boosting current

Figure 3 shows a plot of the poles and zeros as modeled in Matlab, for a boosting current in the p-stage1, *Iboost,p* being equal to 1/4th the current in the main differential pair, IB ($I_{boost,n}$ was fixed to a scaled version of $I_{boost,p}$. The discussion, while referring to $I_{boost,p}$ hold equally for $I_{boost,n}$).

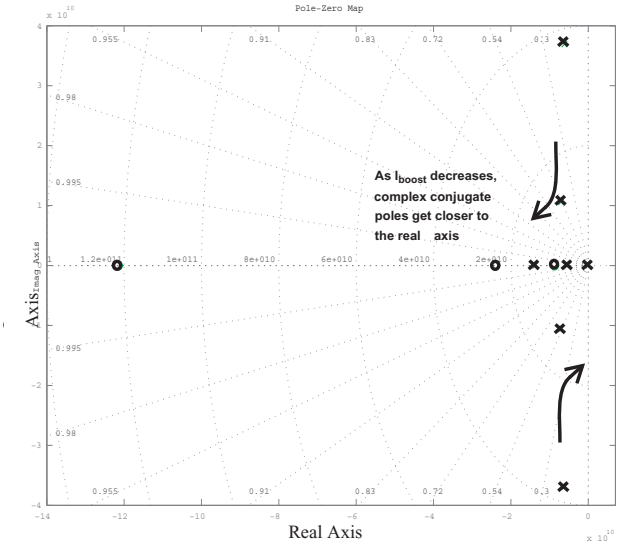

Fig. 3. OTA pole-zero map for $I_{boost,p} = I_{diff}/4$

As the current in the gain-boosting stage decreases, the complex conjugate pairs start to get closer to the real axis until eventually the two complex conjugate poles become real which results in reduced phase margin, ringing in the step response and therefore frequency response degradation of the OTA (Figure 2). Increasing the gain boosting current will, on the other hand, increase the power dissipation.

A tolerable ringing that does not degrade the overall performance of the modulator dictates the choice of the current in the gain boosting stages. A SC common-mode feedback (CMFB) was used in all the above analysis and was chosen due to its low power dissipation. The switches in the SC-CMFB were implemented using transmission gates.

Based on the above analysis, proper system-level modeling allows for careful transistor sizing and biasing choices. With that, low power dissipation could be achieved while still using a single-stage amplifier and while meeting the stringent requirements imposed on the OTA using a single 1.8 V supply and that were synthesized at the system level and summarized in Table 1.

The OTA output swing is though limited to 0.5 V measured differentially. Implications of this limited swing will be discussed further when experimental results are presented.

3.2. Comparator

A CMOS dynamic comparator, with core shown in Figure 4, and a clocked RS latch were used to implement the single-bit quantizer. No pre-amplification stage is used due to the comparator's relaxed offset requirements. To account for hysteresis and the effects of mismatches due to process variations, the comparator was designed to achieve a resolution equivalent to 11 bits, capable therefore of resolving a differential signal of ~880 μV in the current technology.

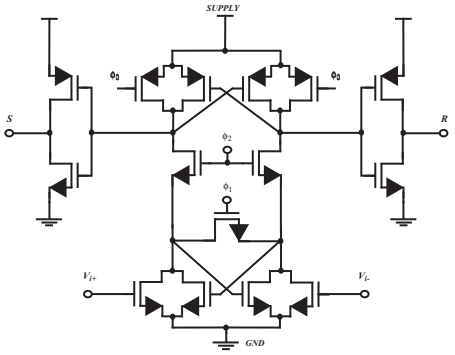

Fig. 4. Comparator core schematics

3.3. Other Blocks

a) Switches

Most designs implemented in deep submicron technologies with minimum feature length less than 0.35 µm and with a supply voltage lower than 3.3 V resort to bootstrapping for the switches. The current paper shows the possibility of implementing the modulators's switches with simple transmission gates. The advantages of using transmission gates is the simplicity of the circuit, and the power and area savings. With proper transmission gate sizing, it is argued that transmission gates suff ce if they are sized to limit their distortion. The experimental results will back up this claim. A design implemented in 0.25 µm technology using a single 2.5 V supply further backs up the current claim. The design achieved 15 bits in dynamic range with simple transmission gates [6]. The switches were implemented using regular transmission gates. The NMOS and PMOS transistors were sized appropriately in order to keep their on-resistance low enough to limit the harmonic distortion [6]. The peak on-resistance of the designed transmission gate was limited to 119 Ω. An on-chip four-phase non-overlapping clock generator was used to clock the switches. Delayed versions of the clocks (together with fully differential implementation) were used to minimize charge injection.

b) Capacitors

While absolute capacitor values are not critical in switched-capacitor designs, matching is of utmost importance since capacitor ratio is primarily responsible for pole/zero placement in the system. Shift of these poles/zeros result in different NTFs and STFs which could possibly result in an increased noise in the band of interest. In some cases, instability might even occur, but is unlikely to happen if the system was designed to be stable under the worst-case variation in capacitor values. In order to achieve best matching, all capacitors were built from a unit-size metal-metal capacitor equal to 125 fF with common centroid techniques adopted. Metal layers 3 through 6 were used, while metal layers 1 and 2 were avoided due to their increased parasitic capacitances with respect to the substrate. Top-metal layers forming the top plate of the capacitor were used to connect to sensitive nodes (such as op amp inputs) due to their lower parasitic capacitances, while lower-metal layers constituting the lower plate of the capacitor were used to connect to less sensitive nodes (such as op amp output nodes). Additional dummy capacitors left unconnected were included around all capacitor arrays to minimize etching effects.

3.4. Full Circuit Implementation

The synthesized block specif cations were mapped into a fully differential SC circuit with capacitor values and modulators' analog coeff cients (given by the capacitor ratios) shown in Figure 5. The digital error cancellation block used to convert the outputs of the three stages into a single fourth-order noise shaped signal was implemented in software with digital coeff cients directly deduced from the analog coeff cients with relationships between the analog/digital coeff cients found in [5]. The SC circuit was then mapped into the IC shown in Figure 6, using a 0.18 µm, single-poly, 6-metal digital CMOS process.

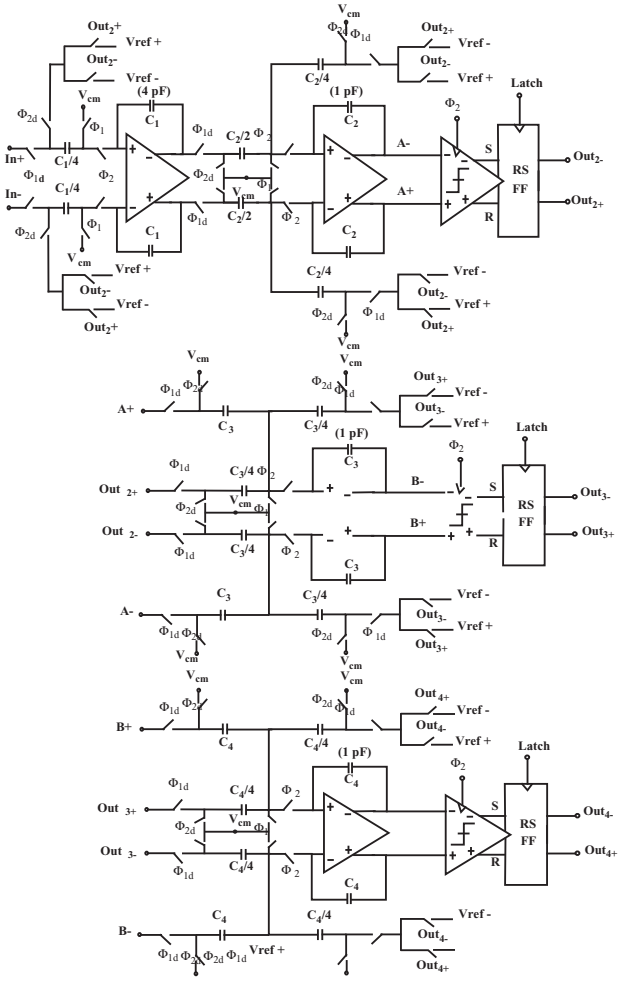

Fig. 5. Three-stage (2-1-1) SC-implementation

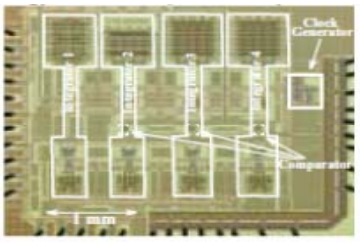

Fig. 6. IC microphotograph

4. EXPERIMENTAL RESULTS

In order to evaluate the performance of the IC, a custom-made four-layer PCB was designed. Separation of analog and digital planes, de-coupling capacitors and voltage regulation for the supply voltage lines were included. The differential input was generated using a Teradyne A567 mixed-signal tester and the clock using a high-quality Hewlett Packard pulse generator model number 81130A. The measured dynamic range (Figure 7) was 12.6 bits of dynamic range where dynamic range is def ned as the difference between the two input levels for which SNDR ≥ 0 dB. The distortion is higher than predicted; the measured total harmonic distortion was 62 dB for a 0.6 V p-p sine wave. This could be explained by the fact that the DAC reference voltages, Vref+ and Vref- were set to full scale (1.8 V and 0 V respectively). The input of the OTA was designed to handle a large swing. The output, however, had a swing that was limited to ~ 0.5 V. On the other hand, shrinking Vref+ and Vref-from full scale to 1.3 V and 0.5 V, respectively, resulted in a decrease in the total harmonic distortion at the expense of an earlier saturation in the input level. This in turn caused a decrease in the peak SNR. Table 2 summarizes the IC measured specif cations.

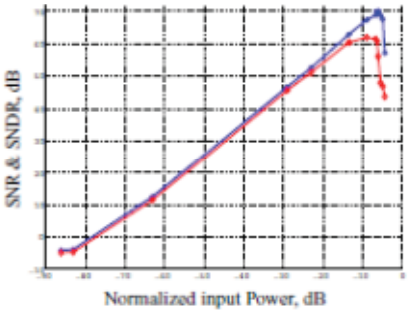

Fig. 7. Measured dynamic range

Table 2

Summary of measured specif cations

Technology / Supply	0.18 µm CMOS / 1.8 V
Power Dissipation	18.8 mW
(V_{ref+}, V_{ref-}) / Input Range	(1.8 V, 0 V) / 1.5 V_{p-p}
f_s, *OSR*, Output Nyquist Rate	50 MHz, 24, ~2 MS/s
DR*, Peak *SNR*, Peak *SNDR	77.6 dB, 70 dB, 62 dB

5. MODULATOR COMPARISON

To evaluate the performance of the modulator with experimental results presented in the previous section in the context of some state-of-the-art lowpass ΔΣMs integrated circuits published in the literature, a f gure of merit, FM is introduced in [5] and is def ned as $FM = P / (2^b \cdot BW)$, where b is the bit-resolution, BW is the output rate, and P is the power dissipation. This f gure of merit could be used to classify the performance of the modulators where a lower FM corresponds to a more performing modulator. A plot of FM as a function of supply voltage is shown in Figure 8.

The designs shown in Figure 8 were chosen among many state-of-the-art implemented in different technologies and using a variety of supply voltages, due to their lowest achieved f gure of merit FM.

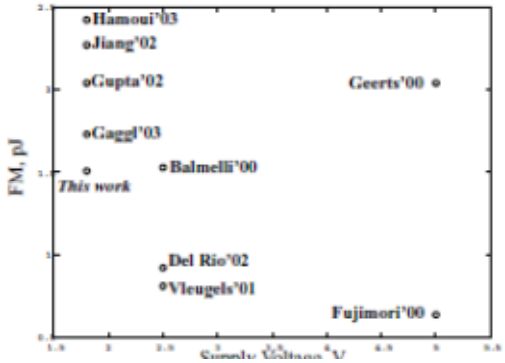

Fig. 8. Performance comparison of some published state-of-the-art ΔΣMs

With this criteria, the modulator implemented ranks well among the best modulators published to date. In terms of supply voltage used, the modulator uses the lowest supply voltage for the modulators' analog core and dissipate the lowest power among the output rates exceeding 2 MS/s.

6. CONCLUSIONS

We have presented the implementation and experimental results of a single-bit ΔΣ ADC in 0.18 µm, single-poly, 6-metal CMOS technology. Minimum power dissipation was achieved through careful system-level modeling and synthesis of circuit specif cations which proved eff cient. A widely adopted f gure of merit reveals the superiority of the achieved performance of the modulator, placing it among the top published to date according to the open literature. Using a single 1.8 V supply, the modulator consumes the lowest power dissipation among the modulators of its class where the output rate exceeds 2 MS/s.

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