CONTENT
Vol. 7. No. 3-2021

Published bi-monthly since 2015.

ISSN 2664-066X (Print)
ISSN 2664-0678 (Online)

Publisher
Institute of Radio and Information Systems (IRIS), Vienna, Austria

Address:
1010 Wien, Austria,
Ebendorferstrasse 10/6b
media-publisher.eu/
synchroinfo-journal

CFA BASED UNIVERSAL BIQUAD FILTER

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DOI: 10.36724/2664-066X-2021-7-3-2-5

ABSTRACT

A universal biquad filter using current feedback amplifiers (CFA) as active devices and a canonical number of capacitors is presented. It realizes the classical feedforward structure through the use of grounded capacitors and MOS transistors, which permit a full integrability. The proposed circuit has attractive characteristics, as the possibility to electronically control the transfer function coefficients and the possibility to be directly inserted within cascaded configurations. The theoretical analysis of the circuit is followed by some PSPICE simulation results in agreement with the theoretical findings. In this paper a universal fully integrable biquad using CFAs as active devices and a canonical number of capacitors is presented. It realizes the classical feedforward structure [3] through the use of grounded capacitors and MOS transistors. The presence of grounded capacitors makes the proposed circuit absorb shunt parasitic capacitances. All the possible kinds of responses can be realized, while in the biquad reported in [2] only the low-pass and band-pass responses can be obtained. The numerator and denominator coefficients of the voltage transfer function of the proposed biquad can be electronically controlled by acting on the gate voltages of the MOS transistors of the circuit. Moreover the presented structure has a low-impedance output and then it can be cascaded without additional buffers.

KEYWORDS: *Analog circuits, continuous-time filters.*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

I. Introduction

Continuous-time filters realizable in fully integrated form continue to receive considerable attention. The techniques appeared in literature in the last years are generally based on the use of active devices alternative to the classical operational amplifier, as, for example, the operational transconductance amplifier (OTA) and the second generation current conveyor (CCII). Until now a relatively little attention has been given to the use of the current feedback amplifier (CFA) in the realization of fully integrated continuous-time filters. The CFA is an amplifier exploiting a circuit topology that emphasizes current mode operation, which is inherently much faster than voltage mode operation [1]. Differently from classical op amps, whose dynamics are limited by the gain-bandwidth product and slew rate, CFAs deliver high bandwidth and slew rate. An example of fully integrated continuous-time filter based on the use of the CFA is reported in [2], where a Tow- Thomas biquad containing capacitors and MOS transistors is presented.

The circuit has been simulated with PSPICE and the simulation results agree with the theoretical analysis.

II. Circuit description

A classical biquad with op amps, resistors and capacitors is the feedforward circuit [3]. The goal is to obtain a fully integrable version of this biquad by using CFAs instead of classical op amps and by replacing the resistors of the corresponding RC circuit with suitable configurations of MOS transistors as the MRC. The MRC (MOS Resistive Circuit), shown in Fig. 1, is a cell constituted by four matched MOS transistors operating in nonsaturation region, with gate voltages equal two by two, which allows to completely cancel the channel resistance nonlinearities of MOS transistors [4].

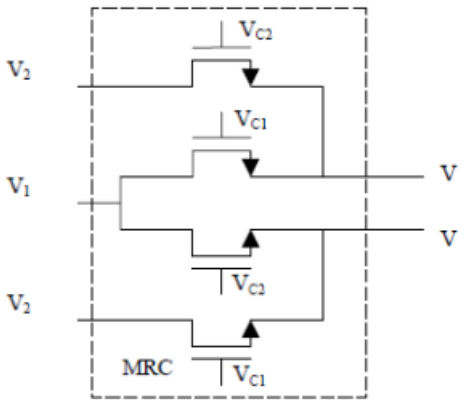

Fig. 1. MRC circuit

In Fig. 2 the fully integrable feedforward biquad is shown. The transfer function is obtained by proceeding in the following way. An ideal model for the CFA is considered, in which the current at the input node Y is zero, the current at the input node X is equal to the current at the internal node Z, the voltages relevant to the nodes Y and X are equal and a unity gain buffer is placed between the internal node Z and the CFA output, so making ideally null the output impedance (this feature permits the direct insertion of the proposed circuit in cascaded configurations). For what concerns the MRC, by supposing, without loss of generality, to use n-channel MOS transistors, the channel current ID in nonsaturation region can be written as follows:

$$I_D = F(V_D, Vc) - F(V_S, V_C)$$

where V_D, V_S and V_C are the drain, source and gate voltages respectively. By exploiting the property that $F(V_A,V_B)$-$F(V_A,V_C) = 2KV_A(V_B-V_C)$ [4], where K is a constant depending on the implementation characteristics of the MOS transistors [4], a routine analysis as in [2] yields the following expression for the transfer function:

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{K_2}{K_8}\frac{(V_{C7}-V_{C8})}{(V_{C5}-V_{C6})}(s^2+As+B)}{s^2+\frac{2K_7}{C_1}(V_{C4}-V_{C3})s+\frac{4K_3K_4K_5(V_{C10}-V_{C9})(V_{C12}-V_{C11})(V_{C14}-V_{C13})}{K_8C_1C_2(V_{C5}-V_{C6})}}$$

$$A=\frac{2K_7}{C_1}(V_{C4}-V_{C3})+\frac{2K_1K_3(V_{C9}-V_{C10})(V_{C2}-V_{C1})}{K_2C_1(V_{C7}-V_{C8})}$$

$$B=\frac{4K_3K_5K_6(V_{C9}-V_{C10})(V_{C14}-V_{C13})(V_{C6}-V_{C5})}{K_2C_1C_2(V_{C7}-V_{C8})}$$

The K_i coefficients, with i=1....6, are relevant to the corresponding MRCi, while K_7 is relevant to the two matched MOS transistors with gate voltages VC3 and VC4 and K8 is relevant to the two matched MOS transistors with gate voltages V_{C5} and V_{C6}. In order to obtain stability, $(V_{C4}-V_{C3})$ and $[(V_{C10}-V_{C9})(V_{C14}-V_{C13})(V_{C12}-V_{C11})]/(V_{C5}-V_{C6})$ must be positive. The transfer function coefficients can be orthogonally adjusted by acting on the gate voltages. To this end, if depletion transistors are used, it is possible to give a zero value to the gate voltages, because this kind of MOS can accept positive, zero or negative gate voltages. On the other hand, if enhancement transistors are used, the DC level of the signals has to be shifted for proper operation [5]. Furthermore, by suitably choosing the gate voltage differences and K_i values, all the kinds of transfer functions can be obtained, both inverting and noninverting. For example:

for the low-pass transfer function the coefficient of s^2 is set to zero when $V_{C7}-V_{C8} = 0$ and, consequently, the coefficient A is set to zero when $V_{C2}-V_{C1} = 0$;

for the band-pass transfer function the coefficient of s^2 is set to zero when $V_{C7}-V_{C8} = 0$ and the coefficient B is set to zero when $V_{C16}-V_{C15} = 0$;

for the high-pass transfer function the coefficient B is set to zero when $V_{C16}-V_{C15} = 0$ and the coefficient A is set to zero by suitably acting on $V_{C2}-V_{C1}$.

Finally for the presented circuit, considering that the terms $2K_i(V_{Cj}-V_{Cr})$ represent conductances [2, 4],

the sensitivities of the transfer function coefficients, with respect to the components, are within the range $0 \leq |S| \leq 1$ and, thus, are quite low.

III. Simulation results

In order to verify the obtained theoretical results, the circuit in Fig. 2 has been simulated with PSPICE. The K value depends on the physical characteristics of circuit in Fig. 2 is shown. The curves are referred to two different values of ω_p obtained by varying V_{C12}-V_{C11}:

V_{C12}-V_{C11} = 1V ($\omega_p = 10^5$ rad/sec, Qp = 5) for the curve marked ◊

V_{C12}-V_{C11} = 4V ($\omega_p = 2 \cdot 10^5$ rad/sec, Qp = 10) for the curve marked Δ.

The other gate voltage differences are the following:

V_{C7}-V_{C8} = V_{C2}-V_{C1} = 0
V_{C5}-V_{C6} = V_{C10}-V_{C9} = V_{C14}-V_{C1}3 = 1V
V_{C4}-V_{C3} = 0.2V V_{C15}-V_{C16} = 1V.

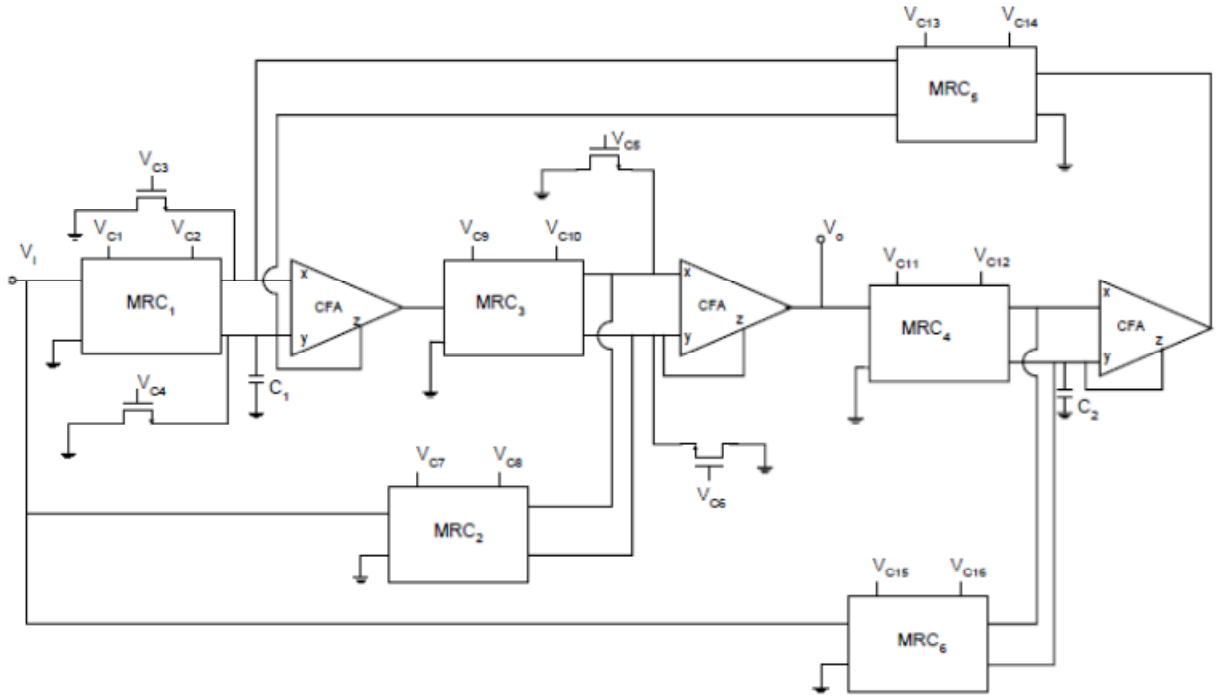

Fig. 2. Universal biquad with CFAs

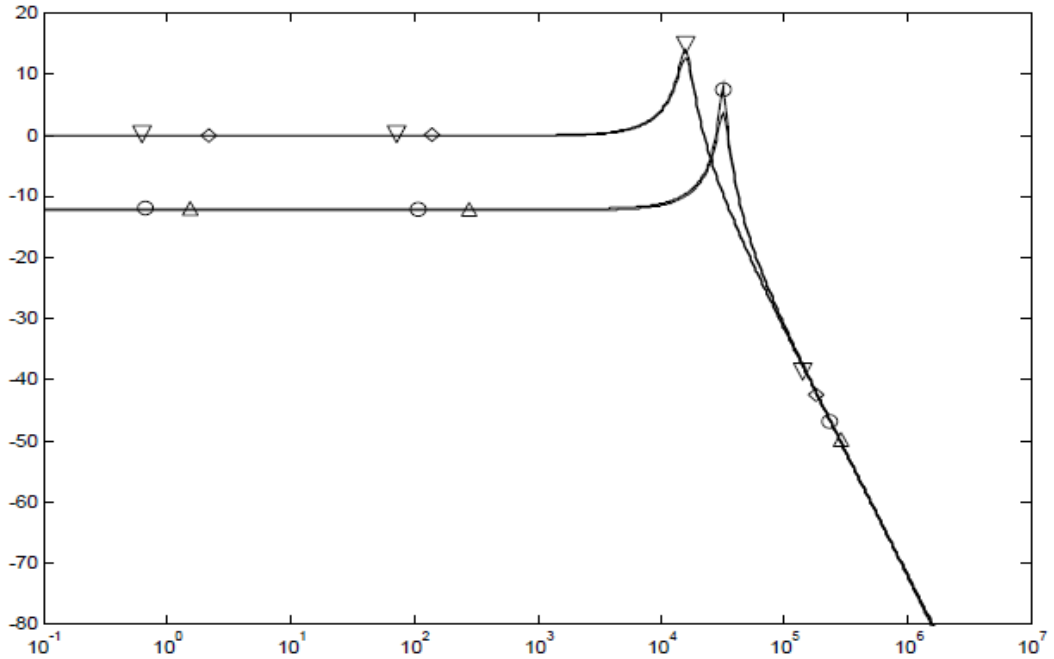

Fig. 3. Gain for a low-pass response of the circuit in Fig. 2: ◊ ∇ V_{C12}-V_{C11} = 1V, Δ O V_{C12}-V_{C11} = 4V (◊ Δ AD844 SPICE model ∇ O CFA ideal model)

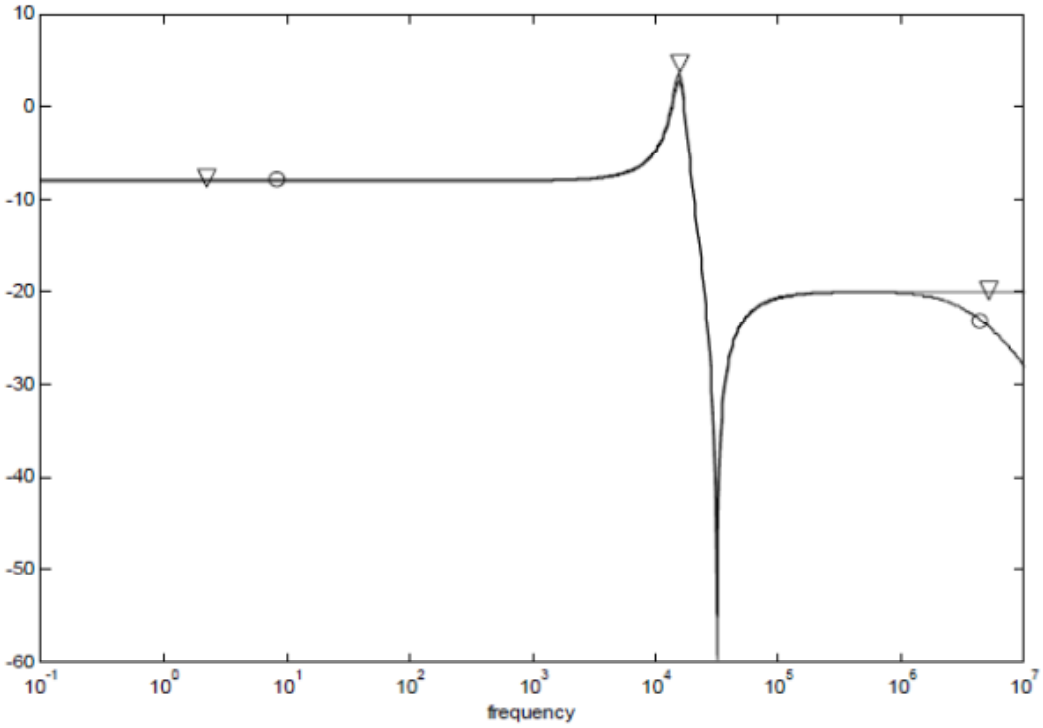

Fig. 4. Gain for a low-pass notch response of the circuit in Fig. 2
(O AD844 SPICE model ∇ CFA ideal model)

In Fig. 4 the gain (dB) for a low-pass notch response is shown. The gate voltage differences are the following:

V_{C5}-V_{C6} = V_{C10}-V_{C9} = V_{C12}-V_{C11} = V_{C14}-V_{C13} = 1V
V_{C2}-V_{C1} = 0.02V V_{C4}-V_{C3} = 0.2V
V_{C15}-V_{C16} = 0.4V V_{C7}-V_{C8} = 0.1V

As a consequence ω_p = 105 rad/sec, ω_z = 2·105 rad/sec and Q_p = 5.

The simulated frequency responses agree with theory.

Conclusions

A universal biquad using current feedback amplifiers as active devices and a canonical number of capacitors has been presented. It realizes the classical feedforward structure through the use of grounded capacitors and MOS transistors, which permit a fully integrability. The circuit offers the following advantages: electronic control of the transfer function coefficients, cascadability, low sensitivity, only grounded capacitors. Finally the simulation results confirm the theoretical analysis.

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SIMULTANEOUS STRAIN AND TEMPERATURE MEASUREMENT USING COMBINED FIBER AND FIBER BRAGG GRATING SENSORS

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DOI: 10.36724/2664-066X-2021-7-3-6-10

ABSTRACT

We propose here a new technique for simultaneous strain and temperature measurement using a Fiber Bragg Grating sensors. This technique employs an interferometric detection using two Fiber Bragg Gratings. A fiber Bragg grating is used as a reference while another fiber Bragg grating and a length of a bare fiber are used as the two sensing elements. As the temperature and strain change, the length of the sensing elements, (Fiber and Fiber Bragg Grating) change. These changes result in a phase and wavelength shifts. To measure these effects we use a Folded Mach Zhender interferometer, and a detection system made out of two photodiodes and data processing system. The sensitivity and dynamic range are analyzed and presented.

KEYWORDS: *Fiber Bragg Grating sensors, optical fiber sensors, wavelength detection*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

Introduction

Optical fiber sensors became devices of choice for many applications over the years. Fiber Bragg Gratings (FBG) are of interest for a variety of sensing applications [1] and in the development of novel all-fiber optical devices such as stop-band and band-pass filters [2], wavelength taps and Fabry-Perot filters [3], strain sensing in smart structures and composite materials [4].FBG sensors are currently the focus of considerable research effort. They are particularly well suited for measuring strain in smart structures [5], and temperature [6]. However, undesirable temperature (or strain) sensitivity of the fiber grating sensor may complicate its application as strain (or temperature) gauge.

As the strain and the temperature are tightly dependent of each other, it is difficult to differentiate between the effects of changes in them. A variety of sensors were proposed to measure both quantities simultaneously. Thermal effect can be well compensated using a pair of fiber gratings in a certain configuration [7]. Two different types of photogenerated fiber grating, namely, a fiber Bragg grating and a fiber polarization-rocking filter [8], the method relies on the different dependencies of the fiber refractive index and birefringence on strain and temperature. It has been suggested that temperature can be measured and compensated using a second grating element contained within a different material and placed in series with the first grating element [9]. The problem of discriminating between strain and temperature has been tackled by use of two Bragg gratings written on the same fiber and operating at different wavelengths [10].

It has been demonstrated that the use of interferometric detection of the phase change or the wavelength shift of Fiber Bragg Grating sensors can yield very high sensitivity of grating temperature or strain. One remaining issue is the separation of the strain-induced wavelength shift from that induced by temperature changes. In dual measurand techniques, strain and temperature are determined from measurement on a "pair of sensors" which are both sensitive to strain and temperature, but have different characteristics.

In this paper, we suggest a novel technique to resolve these two effects dependencies.

We propose here a new technique for simultaneous strain and temperature measurement using a Fiber Bragg Grating sensors. This technique employs an interferometric detection using two Fiber Bragg Gratings. A fiber Bragg grating is used as a reference while another fiber Bragg grating and a length of a bare fiber are used as the two sensing elements.

As the temperature and strain change, the length of the sensing elements, (fiber and FBG), change. These changes result in a phase and wavelength shifts. To measure these effects we use a Folded Mach Zhender (FMZ) interferometer, and a detection system made out of two photodiodes and data processing system. The sensitivity and dynamic range are analyzed and presented.

Theoretical considerations

In this paper, we present a method by which both temperature and strain can be unambiguously determined when they are applied onto the fiber. The FBGs interferometer is used to measure simultaneously these effects by using two identical gratings at room temperature and without strain applied to them.

The setup arrangement used to simultaneously measure strain and temperature using FBGs is shown in Fig.1. Light from a broadband source is coupled into an interferometer with two arms using two FBGs, one arm is used as reference and the second (composed of a grating and a fiber) is used as a sensing arm. Light reaches from the broadband source and partially reflected by the FBGs. The light reflected from FBG1 and FBG2 is at wavelengths λ_1 and λ_2, respectively. In the case of no change in either temperature or strain, λ_1 and λ_2, will be identical.

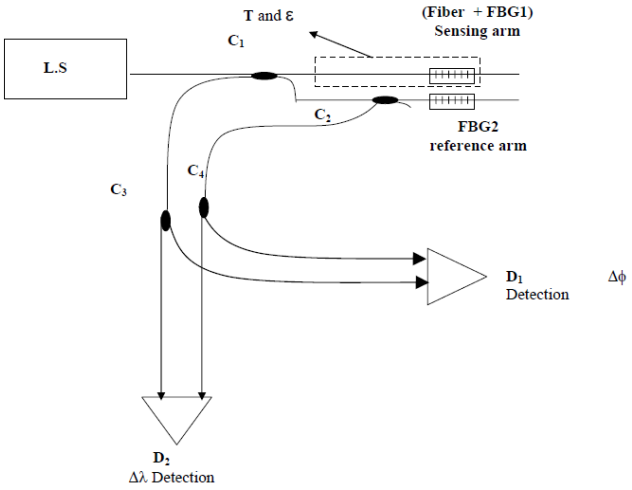


Fig. 1. Fiber Bragg Grating sensor system with sensing (Fiber + Grating) and reference grating elements, and interferometric phase change and wavelength detection

Since the temperature and strain, affect the sensing arm (fiber and grating), this leads to a change in the properties of the fiber and grating, this results in a phase and wavelength shift. If the temperature and/or strain change around the sensing arm the λ_1 will shift accordingly. The waves reflected from both Bragg gratings are combined by the couplers C_1 and C_2, and conveniently separated by using two couplers C_3 and C_4. Light from C_3 and C_4 was split and four waves were launched on two detectors D_1 and D_2. D_1 is used to detect a phase change $\Delta\phi$ and D_2 is used to detect the Bragg wavelength shift, $\Delta\lambda_b = |\lambda_2 - \lambda_1|$.

The corresponding phase change sensitivity due to the temperature and strain effects on the bare fiber is given by,

$$\Delta\phi/\phi = (1/n\ \partial n/\partial T + 1/L\ \partial L/L)\ \Delta T + (1/n\ \partial n/\partial \varepsilon + 1/L\ \partial L/\partial \varepsilon)\ \Delta\varepsilon, \quad (1a)$$

$$\Delta\phi/\phi = (1/n\ \partial n/\partial T + \alpha_T)\ \Delta T + +[1 - n^2/2\ (P_{11} + 2P_{12})]\ \Delta\varepsilon, \quad (1b)$$

where n and L are the refractive index and the Length of the fiber, respectively, α_T is the coefficient of thermal expansion, $1/n\ \partial n/\partial T$ is the thermo-optic coefficient, ΔT and $\Delta\varepsilon$ are the temperature and strain applied on the fiber respectively, and P_{11} and P_{12} are the Pockel`s coefficients.

The shift in the Bragg wavelength sensitivity due to the temperature and strain effects on the FBG can be expressed using:

$$\Delta\lambda b/\lambda b = (1/n\ \partial n/\partial T + 1/\Lambda b\ \partial \Lambda b/\partial T)\ \Delta T + + (1/n\ \partial n/\partial \varepsilon + 1/\Lambda b\ \partial \Lambda b/\partial \varepsilon)\ \Delta\varepsilon, \quad (2a)$$

$$\Delta\lambda b/\lambda b = (1/n\ \partial n/\partial T + \alpha T)\ \Delta T + + [\ 1 - n2/2\ (P_{11} + 2P_{12})]\ \Delta\varepsilon, \quad (2b)$$

where Λ_b is the period of the grating.

Eqs. (1) and (2) can be reduced to a set of linear equations in $\Delta\phi$ and $\Delta\lambda_b$ for any applied strain and temperature which is given by:

$$\Delta\phi/\phi = A\ \Delta T + B\ \Delta\varepsilon$$

and

$$\Delta\lambda_b/\lambda_b = C\ \Delta T + D\ \Delta\varepsilon \quad (3)$$

where the temperature change is in ^oC and the strain is in μstrain, A, B, C, and D are constants which depend on thermo-optic, thermal expansion, and Pockel`s coefficients related to the Fiber material and the FBG.

The constants have a numerical values of [11, 12]:

$$A \approx 7.42 \times 10^{-6}\ (^oC)^{-1},\ B \approx 0.52 \times 10^{-6}\ (\mu strain)^{-1}$$

$$C \approx 7.50 \times 10^{-6}\ (^oC)^{-1},\ D \approx 0.78 \times 10^{-6}\ (\mu strain)^{-1}$$

Numerical analysis

To demonstrate the sensor sensitivity to the temperature and strain, we need to calculate $\Delta\phi$ and $\Delta\lambda b$, a set of known strains and temperatures were applied to the sensor.

In this numerical analysis of the linear system, Eq.(3) we examine the phase and wavelength change as a function of one of the variables while fixing the other. The sensitivity, $\Delta\lambda b / \lambda b$, obtained by our method is around of $0.78 \times 10^{-6}\ (\mu strain)^{-1}$. For $\lambda b = 1550nm$, we obtain a wavelength shift $\Delta\lambda b \cong 0.0012nm / \mu strain$.

The phase shift sensitivity, $\Delta\phi/\phi$, is about $0.52 \times 10^{-6}\ (\mu strain)^{-1}$. If the sensing fiber is 0.25 m long, the phase shift $\Delta\phi \cong 1{,}53$ rad / μstrain. The sensitivity can be altered by choosing different lengths of the fiber.

We obtain a wavelength sensitivity about $7.5 \times 10^{-6}\ (^oC)^{-1}$. The wavelength shift for the same λb is

$$\Delta\lambda b \cong 0.0011nm\ (^oC)^{-1},$$

and a phase change $\Delta\phi \cong 1.5$ rad $/^oC$.

The sensitivity can be altered by changing the characteristics of the FBG.

Detection system:

The sensor is used for simultaneously measuring the wavelength shift, $\Delta\lambda b$, of the Bragg wavelength and the phase change, $\Delta\phi$, between two waves. Therefore, double detection was used. The output optical wave from the interferometer can be represented by the electric fields, reflected from the FBGs. These two optical waves can be represented by,

$$E_1 = E_{01}\ e^{j(\omega t + \phi)} \text{ and } E_2 = E_{02}\ j^{(\omega t + \phi 2)} \quad (4)$$

where ϕ_1 and ϕ_2 are the relative phases of the two waves, and ω is the angular frequency.

The output waves are detected as a corresponding current intensity given by

$$I = E.E^*. \quad (5a)$$

where $E = E_1 + E_2$ is the resultant wave, and * is the complex conjugate, the current is given by,

$$I = I_1 + I_2 + (e^{i\Delta\phi} + e^{-i\Delta\phi})\ \sqrt{}\ I_1 I_2, \quad (5b)$$

for the case where, $I_0 = I_1 = I_2$, I becomes

$$I = 2I_0\ [\ 1 + \cos.(\Delta\phi)\ ], \quad (5c)$$

Eq.(5c), provides the relationship between the output current on the detector D1 and the phase change between the two waves which are reflected from the FBGs. Fig.2 represents the plot of the output current as a function of the phase change $\Delta\phi$ of the detector D1. Once the $\Delta\phi$ is known, we have to detect the wavelength shift $\Delta\lambda b$. For this measurement, we use a heterodyne detection, and we calculate the wavelength shifts $\Delta\lambda b$ of the reflected light, induced by the temperature and strain changes in the sensing elements.

The output optical wave from the interferometer can be represented by the electric fields reflected from the FBGs and detected by the detector D_2.

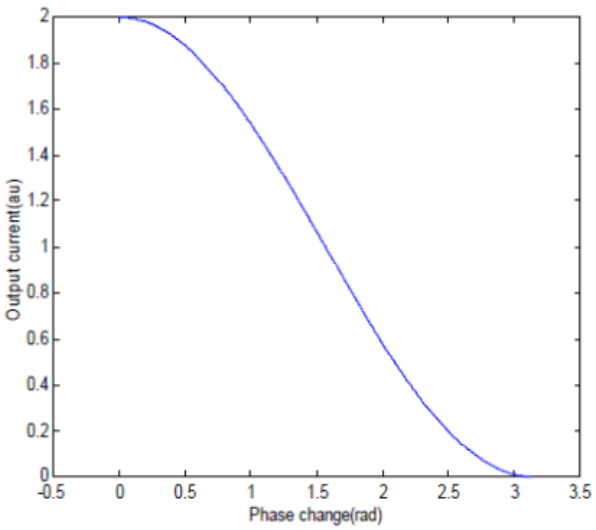


Fig. 2. Output signal obtained on the detector D_1 v.s. the phase change$\Delta\phi$

These two optical waves are given by

$$\Psi_1 = A_1 \cos(\omega_1 t + \phi_1) \text{ and}$$
$$\Psi_2 = A_2 \cos(\omega_2 t + \phi_2) \quad (6)$$

where ω_1 and $\omega 2$ are the angular frequencies of the reflected signals from the reference and the sensing interferometer arms, respectively. ϕ_1 and ϕ_2 are the relative phases of the two signals ($\phi_1 = \phi_2$ and $\omega_1 = \omega_2$, when temperature and strain effects are absent). A_1 and A_2 are amplitudes of the optical waves.

The output waves were detected with a photodiode which acts as a square-law detector. The photo- current generated by the photodiode is given by

$$I(t,T,\varepsilon) = |A_1 \cos(\omega_1 t + \phi_1) + A_2 \cos(\omega_2 t + \phi 2)|^2. \quad (7)$$

In Eq.(7) we dropped the effect of the photodiode responsivity. The photodiode will act as a low-pass filter for the optical frequencies. Therefore, the output current will contain only signals with frequencies lower than that of the optical signal. Therefore the output current is given by:

$$I = A \cos(\Delta\omega_t + \Delta\phi), \quad (8)$$

where

$$\Delta\omega = (\omega_2 - \omega_1), \quad (9)$$

$$\Delta\phi = (\phi_2 - \phi_1). \quad (10)$$

The amplitude A depends on A_1, A_2 and the responsivity of the photodiode.

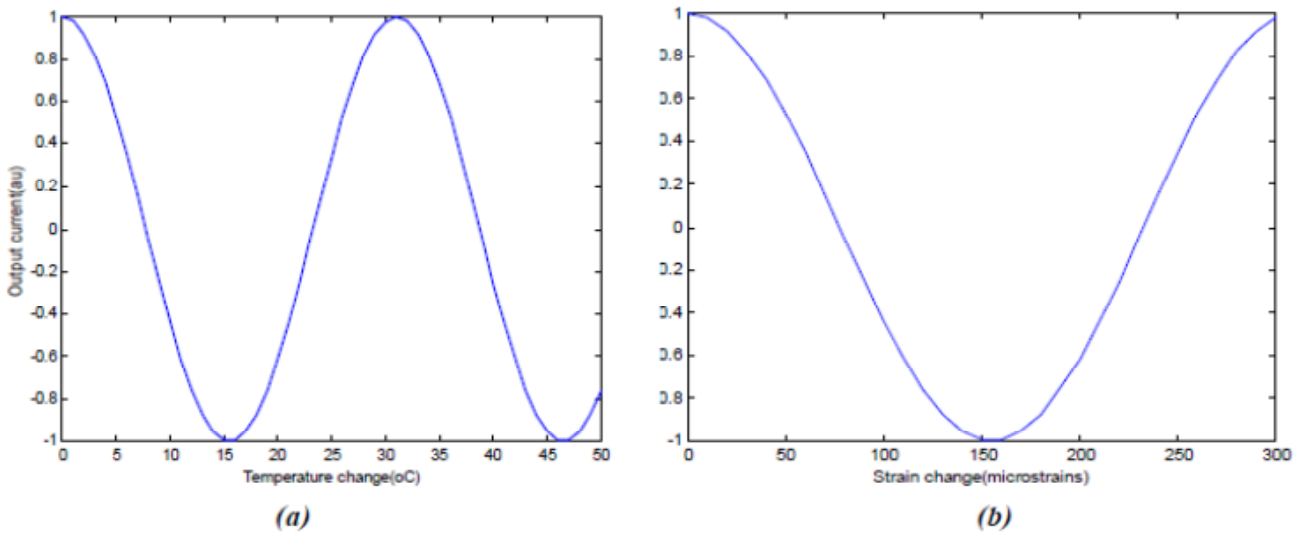
As the temperature and strain change, the frequency, $\Delta\omega$, and the phase, $\Delta\phi$, change accordingly. From Eq.(2b), $\Delta\omega$ can be expressed as a function of ΔT and $\Delta\varepsilon$ by,

$$\Delta\omega = (2\pi C/\lambda_b)[(1/n\,\partial n/\partial T + 1/\Lambda_b\,\partial\Lambda_b/\Lambda_b)\Delta T + (1/n\,\partial n/\partial\varepsilon + 1/\Lambda_b\,\partial\Lambda_b/\partial\varepsilon)\Delta\varepsilon]. \quad (11)$$

and $\Delta\phi$ is known from the Eq.(5b).

The instantaneous output current given by Eq.(7), is plotted as a function of temperature and strain as shown in Fig.(3). We have considered two cases for the strain by keeping temperature change constant, and for the temperature while the strain still constant.

In Fig. 3(a), the dynamic range is 17°C for the temperature and Fig.3(b) shows a dynamic range of 150 μstrains for the strain.



(a) *(b)*

Fig. 3. The output current of detector D_2 as a function of temperature and strain, ***(a)*** strain is constant, ***(b)*** temperature is constant

Conclusions

In summary, we have introduced a fiber optic and FBG sensors that measures simultaneously the temperature and the strain changes in the environment surrounding the sensing arm. The sensitivity and dynamic range are flexible and can be controlled by choosing the length of the bare fiber as well as the characteristics, e.g. grating length and period, of the FBG.

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IRIS ASSOCIATION (INSTITUTE OF RADIO AND INFORMATION SYSTEMS, VIENNA, AUSTRIA)

INTERNATIONAL CONFERENCE

«2021 International Conference «Engineering Management of Communication and Technology» (EMCTECH)

IEEE Conference #53459

20 – 22 October 2021
Vienna, Austria

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Submission dates
Full Paper Submission date: 15 August 2021
Notification of Acceptance date: 30 August 2021
Materials are available in English

http://media-publisher.eu/conference-emctech/call-for-papers/

TIME DOMAIN METHOD FOR THE DETERMINATION OF THE STEADY STATE BEHAVIOUR OF NONLINEAR CIRCUITS DRIVEN BY MULTI-TONE SIGNALS

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DOI: 10.36724/2664-066X-2021-7-3-12-16

ABSTRACT

Time domain methods, while well suited to compute the steady state behaviour of strongly nonlinear non-autonomous electrical circuits, are inefficient if the periods of the forcing signals have a very large minimum common multiple. The solution of the periodicity constraint requires to integrate the differential algebraic equation (DAE) describing the circuit along the T period and this can be a CPU time consuming task. Literature reports several attempts to extend the SH method to simulate circuits driven by multi-tone signals [2] [4] [5]. However, as far as we know, all they suffer of limitations and it is our opinion that an efficient and general extension has not been found, yet. In this paper we present a possible extension that takes its origin from the previous approach reported in [2]. In this paper a modification of the conventional shooting method is presented that tries to overcome the above drawback.

KEYWORDS: *shooting method, harmonic balance, steady state analysis*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications
This research has been supported by the Italian grant MIUR FIRB RBNE012NSW 004

I. Introduction

The harmonic balance method (HB) and the shooting one (SH) are largely used to numerically determine the steady state solution of autonomous and non-autonomous circuits. One main difference between HB and SH is that the former can be adopted to simulate non-autonomous circuits driven by periodic signals whose periods can be very different or even non-commensurate, while, in general, the application of SH to these circuits is convenient only when the minimum common multiple (mcm) of the periods of the driving signals, denoted by T, is a small integer multiple of each of them. This limit of the SH method is due to the fact that its formulation is based on the solution of the periodicity constraint $y_s(T+t)-y_s(t)=0,\ \forall t > t_0$ where $y_s(t)$ is the steady state solution and t is time. The solution of the periodicity constraint requires to integrate the differential algebraic equation (DAE) describing the circuit along the T period and this can be a CPU time consuming task.

Literature reports several attempts to extend the SH method to simulate circuits driven by multi-tone signals [2] [4] [5]. However, as far as we know, all they suffer of limitations and it is our opinion that an efficient and general extension has not been found, yet.
In this paper we present a possible extension that takes its origin from the previous approach reported in [2]. Even though the proposed approach solves some of the drawbacks evidenced in [2], it is still far to be a general method. A main restriction is that it can be applied only to a specific class of circuits that satisfy the assumption that the steady state solution $y_s(t)$ has a spectrum characterised by distinct and suitably separated bands. In this case, we show that through an excursus in the frequency domain it is possible to reformulate the periodicity constraint, so that $y_s(t)$ can be computed only along a small set of time windows each of length Δ and evenly spaced in the circuit working period T. We show that the length Δ of the time window can be chosen as a small fraction of T thus allowing an efficient application of the SH method. Despite the above mentioned restriction, we believe that the proposed method has practical interest, in fact a large number of important circuits for RF applications such as for example mixers, modulators, large band RF amplifiers and travelling waveform amplifiers, belong to this class.

II. Problem formulation

Consider the state equation

$$\begin{cases} \dfrac{dy}{dt}(t) + f(y(t),t) = 0 \quad t \geq t_0 \\ y(t_0) = y_0 \end{cases} \tag{1}$$

where $y(t) : \mathbb{R} \rightarrow \mathbb{R}^{\mathbb{N}}$ is suitably differentiable, $f(y(t),t) : \mathbb{R}^{\mathbb{N}+\mathbb{1}} \rightarrow \mathbb{R}^{\mathbb{N}}$ embeds the periodic driving signals, $t \in \ ^+$ is time and $y_0 \in \mathbb{R}^{\mathbb{N}}$ is the value of the initial condition at the t_0 time instant. Suppose that (1) admits the $y_s(t) : \mathbb{R} \rightarrow \mathbb{R}^{\mathbb{N}}$ steady state solution represented by the series

$$y_s(t) = \sum^{\infty} \left(\varrho_p e^{jp\omega t} - \varrho_p^* e^{-jp\omega t}\right) \tag{2}$$

where $\omega = 2\pi/T$, being T the period of the steady state solution and $\varrho_p \in \mathbb{C}^{\mathbb{N}\times\mathbb{N}}$ are matrices whose entries are the coefficients of the Fourier series and * represents complex conjugation. Being by definition $y_s(t)$ a *solution* of (1), we can write

$$y(t) = y_s(t) + r(t) \tag{3}$$

where the $r(t) : \mathbb{R} \rightarrow \mathbb{R}^{\mathbb{N}}$ function describes how the solution at the current time instant t, that depends on the $y(t_0)$ initial condition, is far from the periodic solution $\widehat{y}_s$.
Our aim is to find the $\widehat{y}_s$ initial condition such that $y(t)$ satisfies the periodicity constraint

$$y(t_0 + T) - y(t) = 0 \tag{4}$$

Adoption of the periodicity constraint (4) requires to integrate (1) at least along one T period but this may require too much numerical effort. To this end we define a new periodicity constraint that solves the above drawback. From (3) we can write

$$\begin{aligned} y(t+\Delta) - y(t) = & \sum_{p=0}^{\infty} \left(\varrho_p e^{jp\omega(t+\Delta)} - \varrho_p^* e^{-jp\omega(t+\Delta)}\right) - \\ & \sum_{p=0}^{\infty} \left(\varrho_p e^{jp\omega t} - \varrho_p^* e^{-jp\omega t}\right) + r(t+\Delta) - r(t) = 0 \end{aligned} \tag{5}$$

where $\Delta \ll T$. We wish to find $y_s(t)$ such that $r(t+\Delta) - r(t) = 0 \ \ \forall t \geq t_0$. Consider the $W_T(\zeta(t), t)$ operator, where $\zeta(t) : \mathbb{R} \rightarrow \mathbb{R}^{\mathbb{N}}$ is a generic function, that removes all components in frequency but only those of the spectrum of $y_s(t)$. The application of $W_T(\zeta(t), t)$ to (5) leads to

$$W_0\left(y(t+\Delta) - y(t), t\right) = W_0\left(r(t+\Delta) - r(t), t\right) = 0 \qquad (6)$$

For example $W_T(\zeta(t), t)$ can be chosen as

$$W_T(\zeta(t), t) = \int_t^{t+T} \zeta(\tau) d\tau$$

but a full T period integration is still required so that it is useless to our purpose.
Introduce now the strong assumption that $\varrho_p = 0$ for $0 \leq L < p < Q$ with $L \ll Q$, $L, Q \in \mathbb{N}$. This means that the spectrum of $y_s(t)$ is characterised by two distinct bands one laying in the frequency range $[0, \nu_L]$ and the other of possibly infinite bandwidth laying above ν_Q. Consider the new version $W_\Delta(\zeta(t), t)$ of the $W_T(\zeta(t), t)$ operator that now zeroes all the components of the spectrum of $\zeta(t)$ laying above the $\nu_\Delta = 1/\Delta$ cut-off frequency

$$W_T(\zeta(t), t) = \int_t^{t+\Delta} w(\tau, t)\zeta(\tau) d\tau$$

where $w(\tau, t) : \mathbb{R} \rightarrow \mathbb{R}^{\mathbb{N}}$ is a suitable windowing function. A good description of the various windowing functions can be found in [3]. Each of them can be considered as a *comb filter* whose zeroes are at frequencies multiple of ν_Δ.

This operator requires to integrate (1) only along the Δ time interval and if we chose $\Delta = T/q$, $q < Q$, this means that Δ can be a small fraction of T. The application of $W_\Delta(\zeta(t), t)$ to (5) leads to

$$\begin{array}{l} W_\Delta\left(\phi(y(t), t, t+\Delta) - y(t), t\right) = \\ \overbrace{\sum_{p=0}^{L}\left(\varrho_p e^{jp\omega(t+\Delta)} - \varrho_p^* e^{-jp\omega(t+\Delta)}\right)}^{\sigma_1(t)} - \\ \overbrace{\sum_{p=0}^{L}\left(\varrho_p e^{jp\omega t} - \varrho_p^* e^{-jp\omega t}\right)}^{\sigma_2(t)} + \\ W_\Delta\left(r(t+\Delta) - r(t), t\right) = 0 \end{array} \qquad (7)$$

The two $\sigma_1(t)$ and $\sigma_2(t)$ series are truncated at the L index since the spectrum of $y_s(t)$ has been zeroed above ν_q. Further they have identical coefficients and, as it can be seen, $\sigma_1(t)$ is a version of $\sigma_2(t)$ delayed by Δ. In the following this aspect is exploited.
We chose $2L + 1$ evenly spaced samples denoted as $t_0, \ldots, t_{2L}$ along the T time interval and apply $W_\Delta(\zeta(t), t)$ to both $y(t_n + \Delta)$ and $y(t_n)$. Define

$$z \equiv \left[\begin{array}{c} W_\Delta\left(\phi_z(t_0), t_0\right) \\ W_\Delta\left(\phi_z(t_1), t_0\right) \\ \cdots \\ W_\Delta\left(\phi_z(t_{2L})\right) \end{array}\right] \quad z_d \equiv \left[\begin{array}{c} W_\Delta\left(\phi_{zd}(t_0), t_0 + \Delta\right) \\ W_\Delta\left(\phi_{zd}(t_1), t_1 + \Delta\right) \\ \cdots \\ W_\Delta\left(\phi_{zd}(t_{2L}), t_{2L} + \Delta\right) \end{array}\right] \qquad (8)$$

the array of samples and its delayed version, respectively, where $\phi_z(\zeta) = \phi(y(\zeta), \zeta, t)$ and $\phi_{zd}(\zeta) = \phi(y(\zeta), \zeta + \Delta, t)$. The $z, z_d \in \mathbb{R}^{\mathbb{N} \times (\mathbb{L}+\ )}$ are column stacked vectors. By applying to z and z_d the Discrete Fourier Transform (DFT), represented by the $\mathbf{F} \in \mathbb{R}^{(\mathbb{L}+\mathbb{1})\mathbb{N} \times (\mathbb{L}+\mathbb{1})\mathbb{N}}$ matrix, the corresponding $\mathcal{Z} = \mathbf{F}z$ and $\mathcal{Z}_d = \mathbf{F}z_d$ approximate spectra are derived ([1]).

We use the word "approximate" since in general $W_\Delta(r(t), t)$, that represents a $\Delta = T/q$ window of T periodic waveform, is not a periodic in the same interval.

However, if $W_\Delta\left(r(t+\Delta) - r(t), t\right) = 0$ were satisfied, we would have $\mathcal{Z}_d = \mathbf{F}z_d = \mathbf{D}(\Delta)\mathcal{Z}$, where $\mathbf{D}(\Delta) \in \mathbb{R}^{(\mathbb{L}+\mathbb{1})\mathbb{N} \times (\mathbb{L}+\mathbb{1})\mathbb{N}}$ is the delay matrix computed by means of DFT. Now it is straightforward to write the equation

$$\mathbf{F}z_d - \mathbf{D}(\Delta)\mathbf{F}z = 0 \ \ \rightarrow \ \ z_d - \mathbf{F}^{-1}\mathbf{D}(\Delta)\mathbf{F}z = 0 \qquad (9)$$

that relates the z_d vector of samples to the z one. By definition (9) represents the *new periodicity constraint*. Finally the substitutions of (8) in (9) yields to the steady state problem

$$\begin{array}{l} \Gamma(\widehat{y}_s) = \left[\begin{array}{c} W_\Delta\left(\phi_{zd}(t_0), t_0 + \Delta\right) \\ W_\Delta\left(\phi_{zd}(t_1), t_0 + \Delta\right) \\ \cdots \\ W_\Delta\left(\phi_{zd}(t_{2L}), t_0 + \Delta\right) \end{array}\right] - \\ \mathbf{F}^{-1}\mathbf{D}(\Delta)\mathbf{F}\left[\begin{array}{c} W_\Delta\left(\phi_z(t_0), t_0\right) \\ W_\Delta\left(\phi_z(t_1), t_1\right) \\ \cdots \\ W_\Delta\left(\phi_z(t_{2L}), t_{2L}\right) \end{array}\right] = 0 \end{array} \qquad (10)$$

whose unknowns are the $y(t_0), y(t_1), \ldots, y(t_{2L})$ initial conditions which are column staked into the $\widehat{y}_s \in {}^{(\ +\ )\times}$ vector. Equation (10) is well formed since it involves $2L+1$ unknowns in $2L+1$ independent equations and ensures that $W_\Delta\left(r(t+\Delta) - r(t), t\right) = 0$, at least at the sampling time instants; note that this does not necessarily imply that $r(t) = 0$.

III. An illustrative example

Consider the scalar equation (11) modelling a non-autonomous circuit driven by P distinct sinusoidal sources

$$\tau\frac{dy}{dt}(t) + y(t) = E + \sum_{p=0}^{P}\frac{a_p}{2}\left(e^{j2\pi\nu_p t} - e^{-j2*\pi\nu_p t}\right) \qquad (11)$$

where $\tau \in \mathbb{R}^+$, $E \in \mathbb{R}$ and $a_p \in \mathbb{R}$, $\nu_p \in \mathbb{R}^+$, with $\nu_p < \nu_{p+1}$, are the amplitude and the angular frequencies of the P sources, respectively. The solution of (11) is

$$\begin{array}{l} y(t) = \phi(y(t_0), t_0, t) = \widehat{\kappa}e^{-t/\tau} + E + \\ \sum_{p=0}^{P}\left(\varrho_p e^{j2\pi\nu_p t} + \varrho_p^* e^{-j2\pi\nu_p t}\right) \end{array} \qquad (12)$$

[1]Since $y(t)$ is not, in general, a scalar function, the $\mathbf{F}$ matrix must be organised so that DFT acts on each component of the $y(t)$ function. Moreover $\mathbf{F}$ is real since real and imaginary parts are on separate rows.

where $\phi(y(t_0), t_0, t)$ is the state transition function and $\rho_p = \dfrac{a_p\,(1 - j\tau 2\pi\nu_p)}{2 + 2\,(\tau 2\pi\nu_0)^2}$. Being $y(t_0)$ the initial condition, from (12) we have

$$\widehat{\kappa} e^{-t_0/\tau} = y(t_0) - E - \sum_{p=0}^{P} \left(\rho_p e^{j2\pi\nu_p t_0} - \rho_p^* e^{-j2\pi\nu_p t_0}\right)$$

the steady state condition for equation (11) is met when $\widehat{\kappa} = 0$ and the steady state solution is

$$y_s(t) = E + \sum_{p=0}^{P} \left(\varrho_p e^{j2\pi\nu_p t} + \varrho_p^* e^{-j2\pi\nu_p t}\right)$$

The $r(t)$ function is represented by the $\widehat{\kappa} e^{-t/\tau}$ term that depends on the initial condition $y(t_0)$. Now by adopting as $w(\tau, t)$ the order 1 Hanning windowing function and applying the resulting $W_\Delta(\zeta(t), t)$ operator to (12) at the generic time instant t_n we have

$$z(t_n) = \underbrace{\int_{t_n}^{t_n+\Delta} \overbrace{\frac{\pi}{2\Delta} \sin\left(\frac{\pi}{\Delta}(\tau - t_n)\right)}^{w(\tau,t)} \phi(y(t_n), t_n, \tau) d\tau}_{W_{\mathrm{HA}}(\zeta(t),t)} \quad (13)$$

From (13) we see that

$$\lim_{(\Delta/\tau)\to 0} \frac{\widehat{\kappa}}{2 + 2\left(\dfrac{\Delta}{\tau\pi}\right)^2} e^{-t_n/\tau}\left(e^{-\Delta/\tau} + 1\right) = \widehat{\kappa} e^{-t_n/\tau} \equiv \widehat{\kappa}_a \quad (14)$$

$$\lim_{(\Delta\nu_p)\to\infty} \frac{1}{2 - 2\,(\Delta\nu_p)^2}\left[\left(e^{j2\pi\nu_p\Delta} + 1\right)\varrho_p e^{j2\pi\nu_p t_n} + \left(e^{-j2\pi\nu_p\Delta} + 1\right)\varrho_p^* e^{-j2\pi\nu_p t_n}\right] = 0 \quad (15)$$

The above limits show that if the integration time interval Δ is suitably chosen with respect to the τ natural frequency and to the ν_p frequencies of the sources, the integral (13) acts like a *low pass filter* that attenuates the amplitude of some "high frequency" components of the spectrum of $y(t)$ [1]. Equation (13) allows us to conveniently reconstruct the samples at the time instants $t_1, t_2, \ldots, t_{2L}$ of the $W_\Delta(y(t), t)$ function that we assume "slowly varying" and approximately characterised by a spectrum composed of the finite number L of harmonics that lie well beyond ν_0. We need thus $2L + 1$ samples in the T period to completely reconstruct $W_\Delta(r(t), t)$. For simplicity suppose that $L = 1$, thus we pick three time instants in the T period: $t_0 = 0$, $t_1 = T/3$ and $t_2 = 2T/3$. The $z(t_0)$, $z(t_1)$ and $z(t_2)$ samples are computed by means of the integral (13) and as described in section II, the components of the $Z(\widehat{f})$ corresponding spectrum are derived through the Fourier transform. In our simple case they are the DC component denoted by Z_{DC} and the component at the $\widehat{\nu} = 1/T$ fundamental frequency, denoted by $Z_1 = Z_1^{\mathrm{R}} + jZ_1^{\mathrm{I}} \in$. In compact form we have

$$\overbrace{\begin{bmatrix} Z_{DC} \\ Z_1^R \\ Z_1^I \end{bmatrix}}^{\mathcal{Z}} = \mathbf{F} \overbrace{\begin{bmatrix} W_\Delta(y(t), t_0) \\ W_\Delta(y(t), t_1) \\ W_\Delta(y(t), t_2) \end{bmatrix}}^{z} \quad (16)$$

where $\mathbf{F}$ is the Fourier matrix. From (16), we can write $W_\Delta(y(t), t) = Z_{DC} + Z_1^R \cos(2\pi\widehat{\nu}t) + Z_1^I \sin(2\pi\widehat{\nu}t)$ that is, we can reconstruct the $W_\Delta(y(t), t)$ function in every time instant. In particular we are able to compute $W_\Delta(y(t), t)$ in three new time instants delayed by the same Δ interval with respect to t_0, t_1 and t_2. In matrix form, we have

$$z_d = \underbrace{\begin{bmatrix} 1 & \cos(2\pi\widehat{\nu}(t_0+\Delta)) & \sin(2\pi\widehat{\nu}(t_0+\Delta)) \\ 1 & \cos(2\pi\widehat{\nu}(t_1+\Delta)) & \sin(2\pi\widehat{\nu}(t_1+\Delta)) \\ 1 & \cos(2\pi\widehat{\nu}(t_2+\Delta)) & \sin(2\pi\widehat{\nu}(t_2+\Delta)) \end{bmatrix}}_{\mathbf{F}_d^{-1}\mathbf{D}(\Delta)} \mathcal{Z} \quad (17)$$

Now, by substituting (16) in (17) we have

$$z_d = \mathbf{F}_d^{-1}\mathbf{D}(\Delta)\mathcal{Z} = \mathbf{F}_d^{-1}\mathbf{D}(\Delta)\mathbf{F}z \quad (18)$$

The entries of the z_d vector in (18) are derived from those of z but, as said in section II, they can be also computed through (13) that represents the $W_\Delta(y(t), t)$ operator, by suitably integrating (12) along the interval $[t_n+\Delta, t_n+2\Delta]$ starting from the same $y(t_n)$ initial conditions adopted to compute z. In other words the entries of both z and z_d depend on the $y(t_0), y(t_1)$ and $y(t_2)$ initial conditions. Once more this is evidenced by substituting (13) in (18)

$$\begin{bmatrix} \int_{t_0+\Delta}^{t_0+2\Delta} w(t)\phi_z(t_0)dt \\ \int_{t_1+\Delta}^{t_1+2\Delta} w(t)\phi_z(t_1)dt \\ \int_{t_2+\Delta}^{t_2+2\Delta} w(t)\phi_z(t_2)dt \end{bmatrix} - \mathbf{M} \begin{bmatrix} \int_{t_0}^{t_0+\Delta} w(t)\phi_z(t_0)dt \\ \int_{t_1}^{t_1+\Delta} w(t)\phi_z(t_1)dt \\ \int_{t_2}^{t_2+\Delta} w(t)\phi_z(t_2)dt \end{bmatrix} = 0 \quad (19)$$

where $\mathbf{M} = \mathbf{F}_d^{-1}\mathbf{D}(\Delta)\mathbf{F}$. Problem (19) is well posed since it is composed of three independent equations involving the three unknowns $y(t_0), y(t_1)$ and $y(t_2)$. If we assume an ideal low pass filtering which implies that limits (14) and (15) hold, we have

$$\begin{bmatrix} \widehat{\kappa}_0 e^{-\Delta/\tau} + E \\ \widehat{\kappa}_1 e^{-\Delta/\tau} + E \\ \widehat{\kappa}_2 e^{-\Delta/\tau} + E \end{bmatrix} - \mathbf{M} \begin{bmatrix} \widehat{\kappa}_0 + E \\ \widehat{\kappa}_1 + E \\ \widehat{\kappa}_2 + E \end{bmatrix} = 0 \implies (\mathbf{1} - \mathbf{M}) \begin{bmatrix} E \\ E \\ E \end{bmatrix} + \left(e^{-\Delta/\tau}\mathbf{1} - \mathbf{M}\right) \begin{bmatrix} \widehat{\kappa}_0 \\ \widehat{\kappa}_1 \\ \widehat{\kappa}_2 \end{bmatrix} = 0$$

where $\mathbf{1}$ is the identity matrix. Since the $\mathbf{M}$ matrix has a unit eigenvalue corresponding to the eigenvector whose entries are all ones, its multiplication by a constant vector gives the same vector as result; therefore $\widehat{\kappa}_0 = \widehat{\kappa}_1 = \widehat{\kappa}_2 = 0$, being $\left(e^{-\Delta/\tau}\mathbf{1} - \mathbf{M}\right)$ invertible.

IV. Simulation results

The first circuit considered is the travelling waveform amplifier shown in fig. 3a; it is driven by the signal $\mathtt{v_{in}}(t) = v_o\,(\sin(2\pi f_1 t) + \sin(2\pi f_2 t))$, where $v_o = 45\,\mathrm{mV}$, $f_1 = 100\,\mathrm{MHz}$ and $f_2 = 102\,\mathrm{MHz}$. The period of the resulting steady state waveforms is 500 ns (mcm of $1/f_1$ and $1/f_2$).

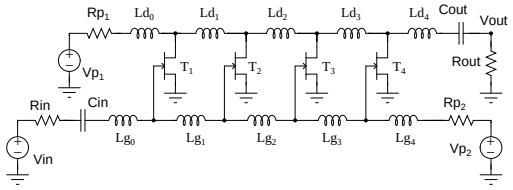

Fig. 3a. The schematic of the travelling waveform amplifier.

A portion of the periodic waveform at the output of the amplifier is shown in fig. 3b; we see that the waveforms computed by the harmonic balance method (HB) and the proposed method (MTS) basically overlap along each time window.

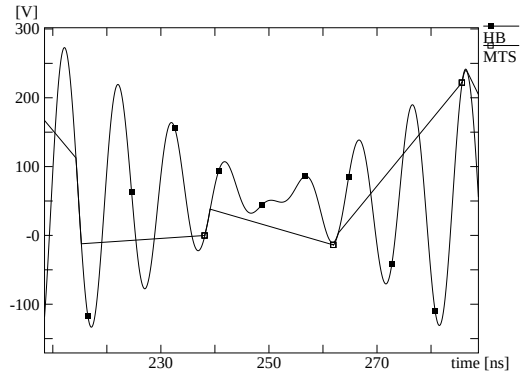

Fig. 3b. A portion of the periodic waveforms at the output of the travelling waveform amplifier.

Locations of time windows employed by MTS (total number equal to 21, corresponding to 10 harmonics, each 1 ns wide) can be easily found since they are "connected" by segments in fig. 3b.

The second circuit considered is the mixer shown in fig. 4a. The local oscillator driving the mixer is represented by the `V1o` independent voltage source that generates the sinusoidal waveform $0.1\sin(2\pi f_{\mathrm{LO}}\,t)$, where $f_{\mathrm{LO}} = 1\,\mathrm{GHz}$. The RF input is modelled by the `Vrf` voltage source that generates the signal $\sin(2\pi f_{\mathrm{RF}}\,t)$, where $f_{\mathrm{RF}} = 1\,\mathrm{GHz} - 100\,\mathrm{MHz}$; the output filter of the mixer, composed of `L2` and `C2`, is tuned at the $f_{\mathrm{IF}} = 100\,\mathrm{MHz}$. Figure 4b shows the output waveforms of the mixer computed by HB and MTS. The MTS one has been obtained by employing 21 time windows each 100 ps wide. Once more we see a good agreement between the waveform computed by HB and the MTS one, even though, in this case, there is a certain phase shift between them.

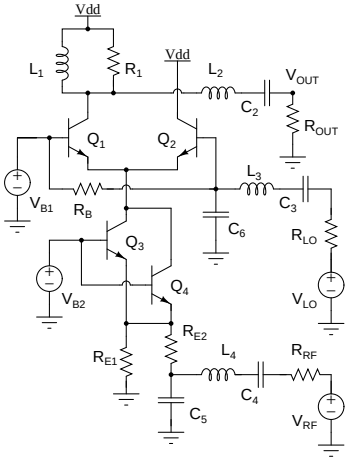

Fig. 4a. The schematic of the mixer.

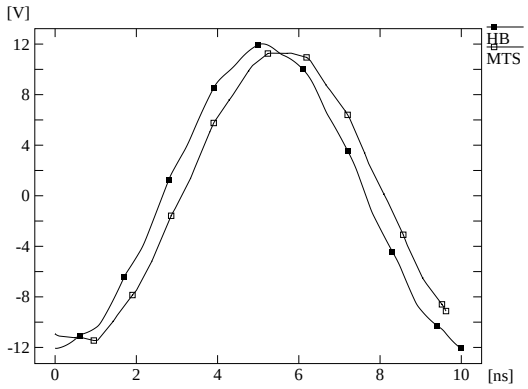

Fig. 4b. The `Vout` output waveform of the mixer.

V. Conclusions and future work

The numerical algorithm presented in this paper can be considered as the first version of an approach to simulate, in the time domain, non-autonomous circuits driven by two tone at different frequencies. As future work, we are going to develop a new version of the algorithm that removes the drawback mentioned in the introduction and increases numerical robustness, since the current version can lead, in some cases, to ill-conditioned or even singular matrices.

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TRAPEZOIDAL CURVES IN WIDEBAND PATCH ANTENNA DESIGN

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DOI: 10.36724/2664-066X-2021-7-3-17-21

ABSTRACT

This paper opens investigations on patch antenna and simple and deformed trapezoidal shape invariants. The simplest and the most compact the antenna is, the most efficient it is and the less it costs. When we aim for a wideband communication, we should design our antennas while taking into account many essential electromagnetic characteristics. This paper studies different patch antenna shapes based on trapezoids. Curves are explored to modify these shapes and to ameliorate the quality of wideband antennas. The moment method is used here as a technique of analyzing (MOM) electric and magnetic fields. Actually, novel invariants in the explored shapes, were underlined in this paper and orient the antenna designer to take care of their dimensions as well as these variables affects closely the bandwidth offered consequently by the designed antenna.

KEYWORDS: *Trapezoid, Curves, Wideband, Design, Patch Antenna, Simulation*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

I. Introduction

In this paper, we try to shape originally our antennas by curved lines. So, we manage these curves as well as we ameliorate antenna reflection coefficient S11. The major aim of this study is to preview the behavior of such antennas and how these non rectilinear shapes are helpful to design wideband antennas. To concretize such idea, we have chosen different shapes as indicated in Fig.1 and Fig. 2. These antennas are designed then simulated using different design tools such as ADS2003 and ANSOFT-Ensemble and our laboratory tools.

We had explored the moment method MOM [1] in order to deduce characteristics of the simulated antennas such as reflection coefficient. We had unified for these antennas the same dielectric: FR4_epoxy (Er=4.4) with 0.794mm as a width (antenna designer could choose this substrate width to get adjusting resonant frequency bands) and used thin copper as conductor to shape the trace of the top and the ground of the antenna. So, simplicity and originality are combined to unveil some secrets of curves in trapezoidal shapes.

Then, we had simulated these different antennas and tried to extract such curves impact on antenna characteristics [2]. First of all, we had distinguished many shape invariants such as radius of the circle in or the circle out (R_out, R_In), L: Length and W: Width of the trapeze, and the couple (LA, WA) as the length and the width of adaptation line fixed respectively to (6mm, 4mm). The second step is that we had defined five dimensions and the best four trapezoidal shapes [3].

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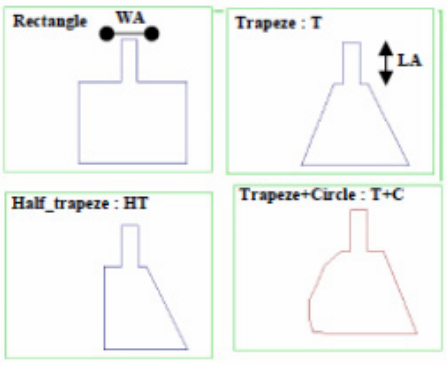

Fig. 1. First set of simulated antennas

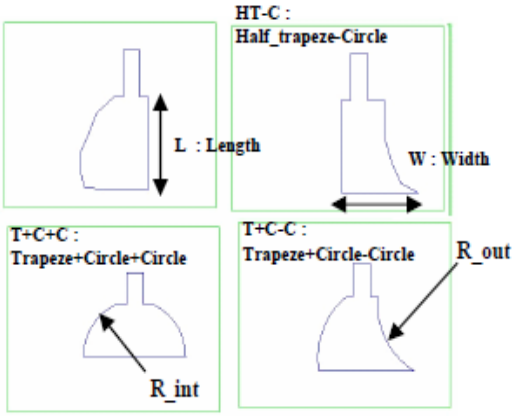

Fig. 2. Second set of simulated antennas

II. Si ation and results

Models and mathematical foundations of this paper were detailed and explored in our previous papers [5, 6] where we had presented the MOM as the explored method to analyze and calculate antenna characteristics [2, 4].

II.1. Shapes' impact [3]

We represent here S11 in dB versus frequency for each couple of antenna in that we compare them by frequency bands from 1 to 20 GHz. Then, we deduce the principal conclusions offered by these simulations. Each time we compare two antenna cases, we should precise the concerned frequency interval [4].

The six next figures From Fig. 3 to Fig. 8 represent the different S11 (dB) of each chosen case (we had unified L=20mm and W=26mm for all the antennas). Each case is a comparison of two antennas. Fig. 3 illustrates how the rectangle is better than the trapeze in the interval (1.3 to 4.5) GHz. However, Trapeze is considered better in the interval (15 to 17) GHz. All the results are below in table 1.

Table 1

Shapes and bands resonance

Shapes/ Intervals(GHz) From To	I_0 1.4 2	I_1 2.4 4.5	I_2 3.2 4	I_3 12 15.8	I_4 12.2 14.8	I_5 15.3 16.8	I_6 16 17.4
Band Width Δ I (GHz)	0.6	2.1	0.8	0.8	2.6	1.5	1.4
Rectangle (Fig.3)	-	-	+	-	-	-	-
Trapeze (Fig.3,4)	-	-	-	-	-	+	-
Trapeze +C–C (Fig.4,5)	+	+	+	-	-	-	+
Trapeze +C (Fig.5, 8)	+	+	+	-	-	-	-
Trapeze –C–C (Fig.6)	+	-	-	+	-	-	-
Trapeze +C+C (Fig.6)	+	-	+	-	+	-	-
Half Trapeze (Fig.7)	-	-	-	-	-	-	-
Half Trapeze +C (Fig.8)	-	-	-	+	-	-	-
Half Trapeze –C (Fig.7)	+	-	+	-	-	-	-

Figure 4 demonstrates how adding positive and negative curved surface to a trapeze, affects positively the quality of the antenna even that surface value remains unchaged in the case of a regular trapeze. Fig. 5 illustrates that adding only one positive-curve (T+C) is better than adding two curves (T+C-C) without chaging the surface of the trapeze. In Figure 7, we see how much negative-curve minimises S11 (dB). However, Figure 8 demonstrates how dividing the trapeze by two has deteriorated the quality of the antenna relatively to the entire trapezes. That why we've get rid of the half trapezes HT antennas in the next section of our simulations.

Fig. 6 compares double positive curves (T+C+C) and double negative curves (T-C-C), the first is a bit better around 4, 5 and 14 GHz. So, adding curves may be a feature that helps the antenna designer to choose the right shape for his application. But with witch dimensions [3]?

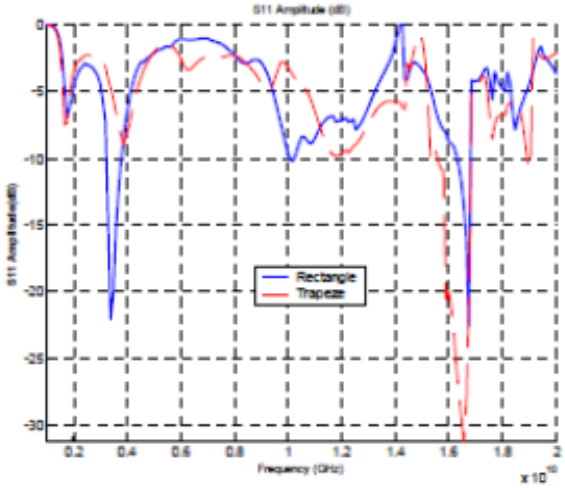

Fig. 3. Reflection coefficient S11 versus frequency Case of Rectangle and Trapeze.

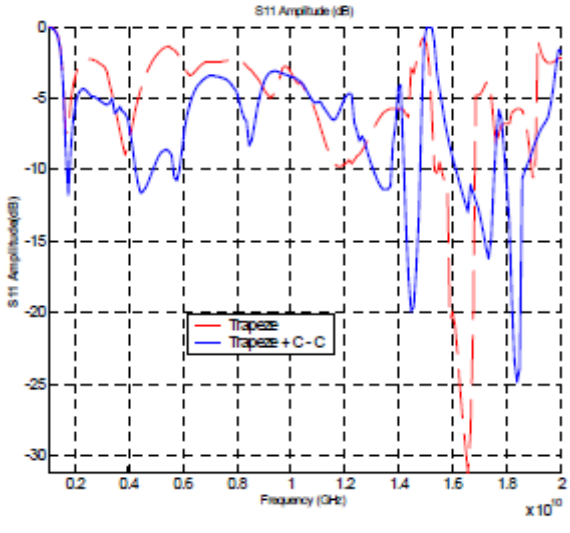

Fig. 4. Reflection coefficient S11 versus frequency Case of Trapeze and T+C-C

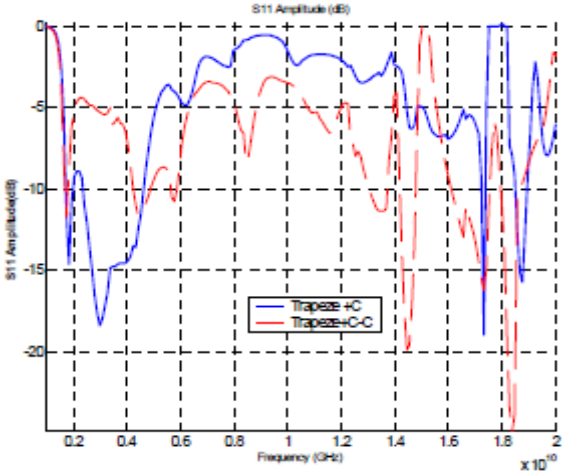

Fig. 5. Reflection coefficient S11 versus frequency Case of T+C and T+C-C.

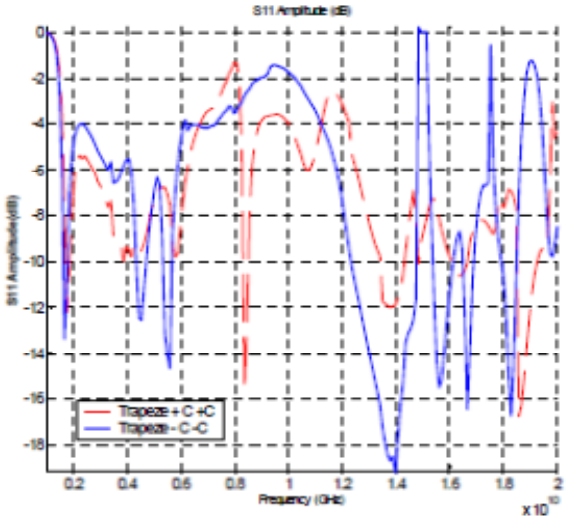

Fig. 6. Reflection coefficient S11 versus frequency Case of T+C+C and T-C-C.

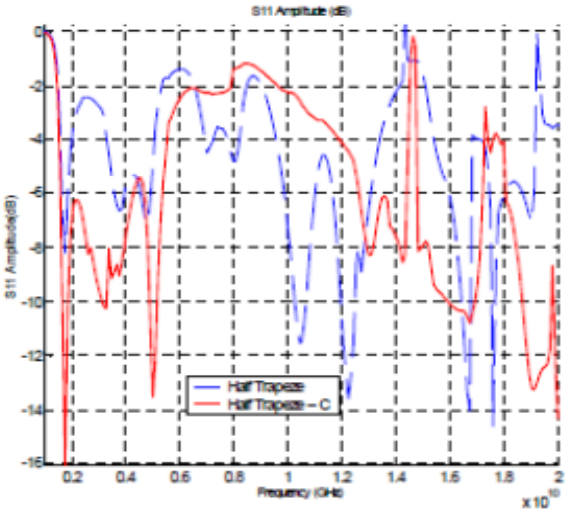

Fig. 7. Reflection coefficient S11 versus frequency Case of HT and HT-C

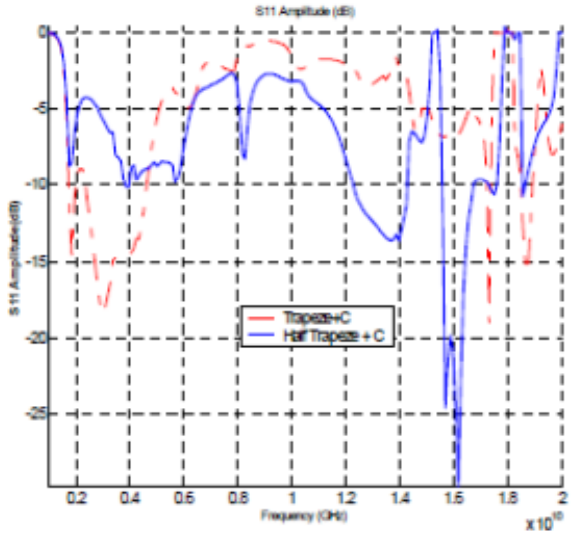

Fig. 8. Reflection coefficient S11 versus frequency Case of T+C and HT+C

II-2. Invariants impact

The first battery of simulations helped us to select some antennas witch we modified dimensions to see if this latter involves any change in the antenna behaviour [4]. Here are the five dimensions (Dim0, Dim1, Dim2, Dim3, and Dim4) applied to these four shapes [1) T+C, 2) T-C-C, 3) T-C, 4) T+C+C]:

(mm)	L	W	R_in	R_out
Dim0:	12	24	12	12
Dim1:	20	35	20	20
Dim2:	20	40	20	20
Dim3:	24	47	24	24
Dim4:	28	52	28	28

Figurs 9-13 are the results of simulations of chosen antennas for several dimensions. Figure 9 illustrates the comparison of the four mentioned antennas in the case of the smallest dimension (Dim0). Two curves added to a Trapeze (T+C+C) has the less reflection coefficient S11 on two widebands around (4.5GHz,-20.74 dB) and (6.44GHz,-28.61 dB).

Whenever the dimension increases frequencies are shifted to the left as S11 decreases or may increases too.

Figure 10 unifies the four antennas around 1.9 ± (0.6, 0.2) GHz, but illustrates that the negative-curved trapeze (T-C) resonates also around 8.7 ± (0.2, 0.2) GHz.

Figure 11 proves how when dimension decreased (from Dim1 to Dim2), (T+C) and (T+C+C) resonate not only around 1.7 ± (0.1, 0.1) GHz but also around 3.4 ± (0.2, 0.2) GHz. And this as a shift to the left of S11 and a bifurcation in two bands instead of one. (T-C-C) resonates also around 5.8 ± (0.2, 0.1) GHz. (T-C) resonates also around 7.8 ± (0.2, 0.1) GHz.

According to Figure 12, (T+C) and (T-C) resonates in many widebands. (T+C) is efficient around 12.9 ± (0.5, 1) GHz and less efficient around 3.7 ± (0.2, 0.2) GHz and 8.6 ±(0.1, 0.1) GHz. (T-C) resonates around 5.6 ± (0.3, 0.2) GHz and less efficient around 7.1 ±(0.2,0.2) GHz. Fig.13 shows how (T+C+C) is the best antenna in this dimension (Dim 4). In that, it resonates around five bands such as 2.4 ±(0.3,0.3) GHz and 3.4 ± (0.1,0.1) GHz.

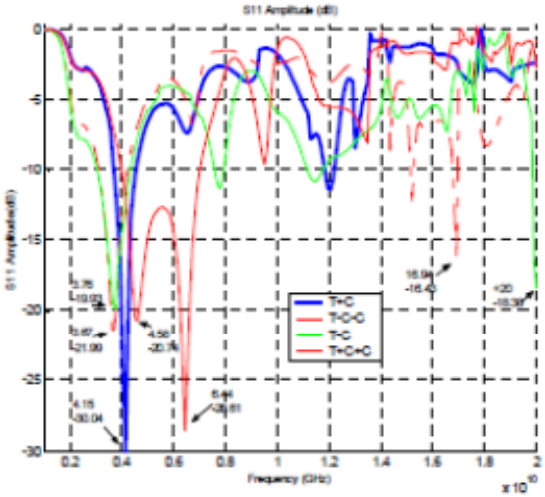

Fig. 9. T+C & T-C-C&T-C & T+C+C (Dim 0)

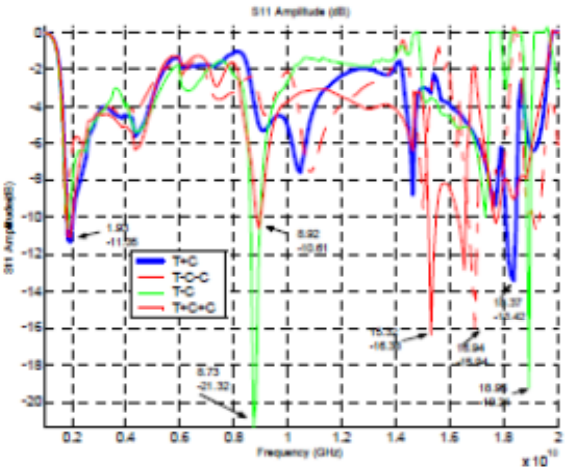

Fig. 10. T+C & T-C-C & T-C & T+C+C (Dim 1)

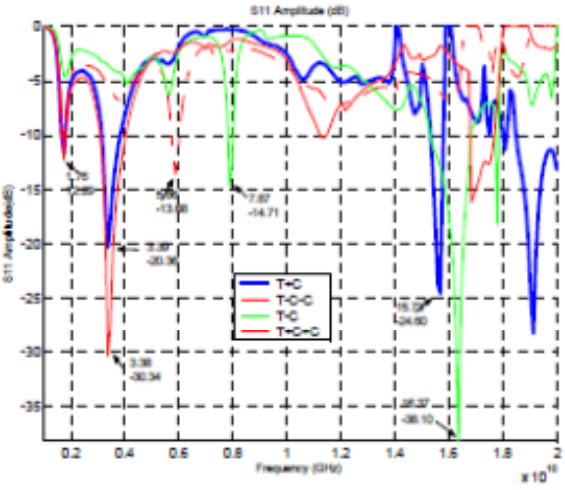

Fig. 11. T+C & T-C-C & T-C & T+C+C (Dim 2)

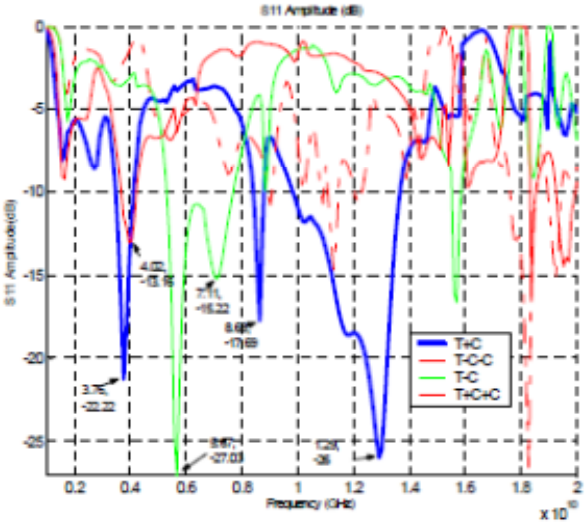

Fig. 12. T+C&T-C-C & T-C&T+C+C(Dim 3)

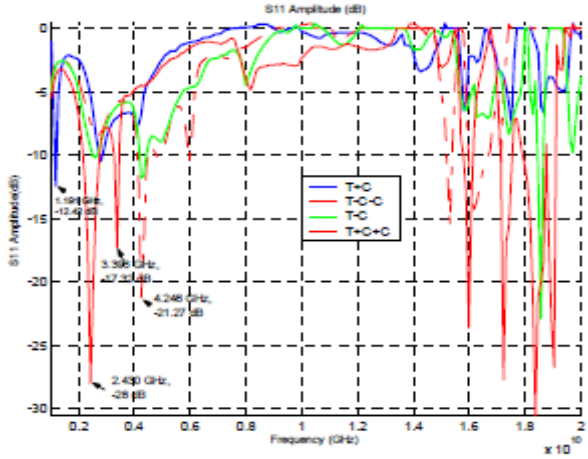

Fig. 13. T+C & T-C-C & T-C & T+C+C (Dim 4)

Conclusion

In order to design more simple antennas, we have realized two simulation batteries based on trapezoidal shapes combined with curves and applied to five chosen dimensions. Results were verified and commented as well as each studied trapezoidal antenna unveiled its caracteristics. This paper opens an old_new axle research on new simple shapes'antenna. However, we are working also on chaotic shapes.

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IMPLEMENTATION OF A REDUCED COMPLEXITY HIGH PERFORMANCE DATA ACQUISITION CHIP USING 0.18 MICRON TECHNOLOGY

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DOI: 10.36724/2664-066X-2021-7-3-22-26

ABSTRACT

Data acquisition (DAQ) in the general sense is the process of collecting information from the real world. For engineers and scientists, this data is mostly numerical and is usually collected, stored and analysed using computers. However, most of the input signals cannot be read directly by digital computers. Because they are generally analog signals distinguished by continuous values, while computers can only recognise digital signals containing only the on/off levels. DAQ systems are therefore inevitably necessary, as they include the translation requirements from analog signals to digital data. For this reason, they have become significant in wide range of applications in modern science and technology [1]. The paper precents the disign of a 12-bit high-speed low-power Data Acquisition (DAQ) Chip. In this paper, the disigns of the building block components are aimed at high-accuracy along with high-speed and low power dissipation. A modifided flash Analog-to-Digital converter (ADC) was used instead of the traditional flash proposed DAQ chip operates at 1 GHz master clock frequency and achieves a sampling speed of 125 MS/s. It dissipates only 64.9 mW of power as compared to 97.2 mW when traditional flash ADC was used.

KEYWORDS: *Data acquisition, High-speed integrated circuits, Integrated circuit design, Analog-to-Digital Converter.*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

I. Introduction

Existing DAQ systems tended to use reasonably fast and accurate ADC, such as SA ADC. These systems can run at maximum 50MHz, providing the maximum data sampling rate of 150kS/s [2, 3]. They were the perfect solution for accuracy applications such as process control and test/measurement applications. However, applications such as high-end video signal processing, high performance wireless communication and power fault analysis [4, 5] require the signal sampling rate approaching 80MS/s. The existing DAQ systems, therefore, cannot fulfil this speed requirement. Out of all conventional ADCs, only flash ADC could provide the sampling speed beyond 100MS/s. However, flash ADC suffers from the main disadvantages of very large die size and high power consumption.

This leads to the need of architectures and circuit techniques enabling DAQ system to attain enhanced performance with reasonable chip area and power dissipation. In this DAQ design, emphasis was put on the reduction of system complexity and power dissipation while achieving a high sampling speed to satisfy current application requirements. The layout of the designed DAQ chip has also been implemented. The results of layout simulation have been back annotated, analysed and presented in this paper.

II. Da Acquisition Design

The typical building blocks of a DAQ system include an analog multiplexer (MUX), Programmable Gain Amplifier (PGA), anti-aliasing filter, Sample-and-Hold circuit (SHC), Analog-to-Digital converter (ADC) and a system controller, as shown in Fig. 1 where the ADC is the key element in the DAQ device.

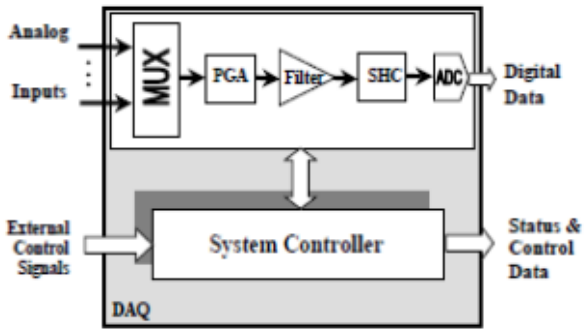

Fig. 1. Block Diagram of a Typical DAQ Chip

3.1. Analog Multiplexer

An analog MUX is one of the most sensitive parts of the design. It is the most responsible device for accurate sampling of multi-input channels. A MUX typically comprises of several switches connecting all of the input channels to the output end of the MU CMOS transmission gate (TG) is typically chosen to implement the switches due to its superior characteristics including high dynamic analog range and clock feedthrough error elimination. For the proposed DAQ system, a 4:1 analog MUX was designed allowing 4 channels to be processed. The binary control word (sel1sel2) selects the input using the following logic expression:

$$v_{out} = v_{in1}(\overline{sel_1}.\overline{sel_2}) + v_{in2}(\overline{sel_1}.sel_2) + v_{in3}(sel_1.\overline{sel_2}) + v_{in4}(sel_1.sel_2) \quad (1)$$

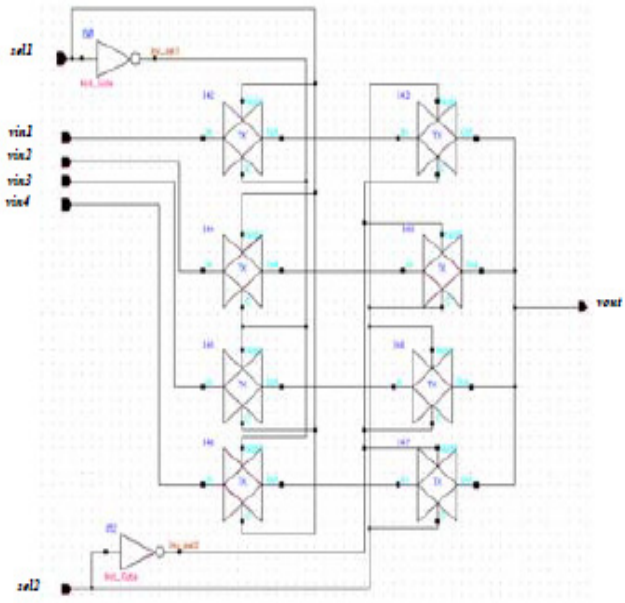

Fig. 2. Schematic diagram of 4:1 M1 MUX

3.2. Programmable Gain Amplifier

It is critical to have a PGA in a DAQ system to boost low-level input signals to maintain the linearity over the entire ADC bandwidth.

Figure 3 presents a PGA using feedback network to achieve high linearity. A current-mode amplifier with fixed equivalent feedback resistances of R_2 can maintain a constant feedback factor, regardless of the input equivalent resistances of R_1. Thus, the amplifier can be optimised for minimal power dissipation with a specific bandwidth [6]. With proper resistor design and transistor sizing, R_1 will be adjusted so that the average current signals in the resistors remain constant, leading to little change of linearity at the PGA's outputs.

Traditional Bipolar and BiCMOS continuous time transconductance filters usually trade off high linearity with increased noise. Similarly, conventional CMOS filters typically do not achieve a high dynamic range. CMOS switched capacitor (SC) filters achieve several advantages over its counterparts. It exhibits improved dynamic range, is more capable of handling large signals, and is capable of being programmable by changing its sampling frequency [7].

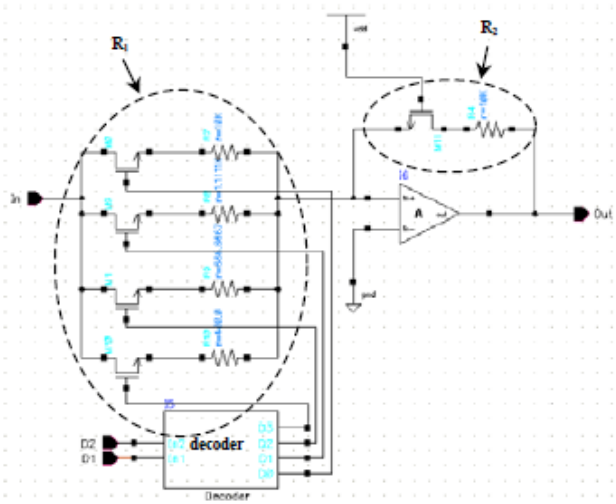

Fig. 3. Schematic Diagram of PGA

Fig. 4 illustrates a SC low pass filter comprising of an inverting integrator and a non-inverting integrator. The transfer function of the filter is described in equation (2). In the design, capacitors C4 and C5 compensate the offset voltage and DC gain error of the OPAM A1 and A2 respectively while capacitor C2 eliminates spikes (providing continuous feedback to the filter).

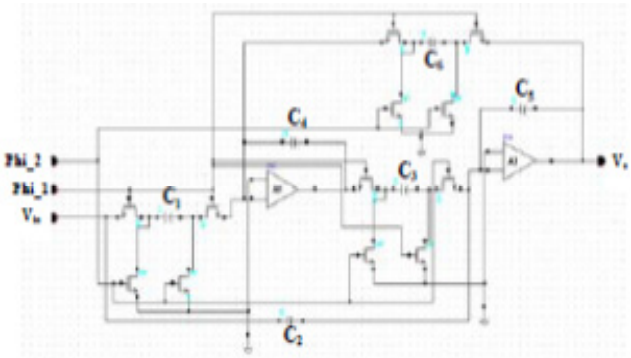

Fig. 4. Switched Capacitor Filter Schematic

$$H(s)=\frac{V_0}{V_i}=-\frac{C_4C_6+4\pi^2f^2f_c^2C_1C_3}{C_4C_5+4\pi^2f^2f_c^2C_2C_3} \qquad (2)$$

3.3. Sample-and-Hold Circuit

SHC is an important building block in DAQ system since the system throughput and accuracy are limited by the speed and precision at which the input is sampled and held.

Figure 5 depicts the schematic diagram of SHC architecture utilised in the proposed DAQ system.

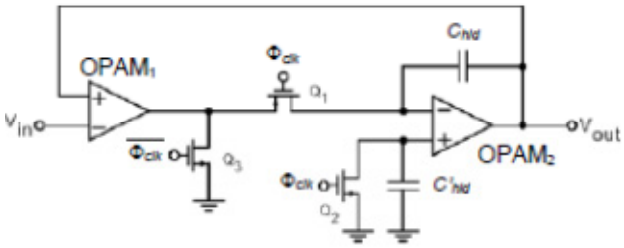

Fig. 5. SHC using feedback loop with compensate capacitor

In this circuit, the sampling switch Q1 is maintained at a virtual ground during the sampling phase and therefore the charge injection error is effectively removed. Also, a supplementary NMOS switch Q2, identical to Q1 and a compensate capacitor *C'hld*, identical to the holing capacitor *Chld* are added to eliminate the clock feedthrough error. This type of SHC, therefore, obtains a superior high-accuracy characteristic.

3.4. Analog-to-Digital Converter

Pipeline ADC consists of numerous consecutive stages, each stage containing a SHC, a low resolution ADC, Digital-to-Analog converter (DAC) and a summing circuit that includes an amplifier to provide gain [8], as shown in Fig. 6.

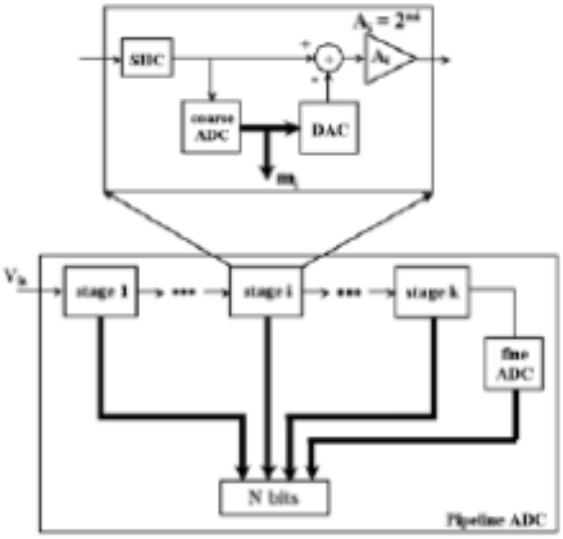

Fig. 6. Pipeline ADC Architecture

Flash ADCs are typically employed as coarse and fine ADCs in a pipeline ADC architecture. However, the major disadvantages of the full flash ADC architectures are high device power consumption, high device complexity and high device input capacitance.

A modified flash ADC [9, 10], as illustrated in Fig. 7, was used instead of the traditional full flash ADC to reduce design complexity and power dissipation.

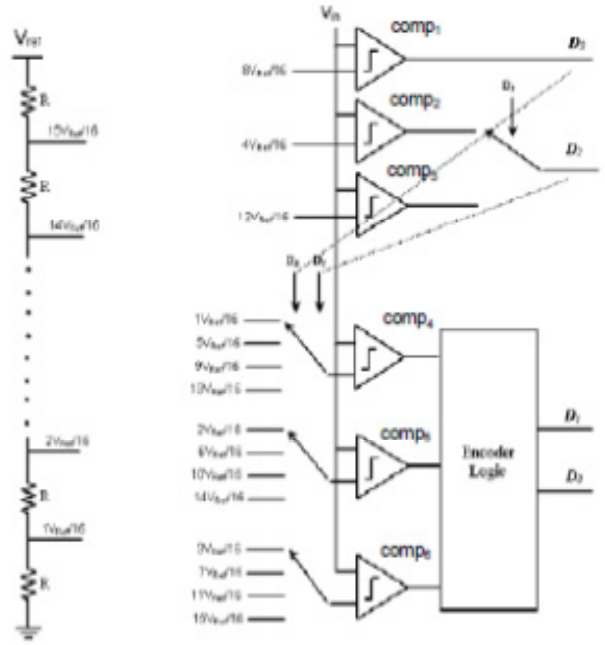

Fig. 7. Four-bit Modified Flash ADC

The modified flash ADC, which utilised an optimised latched-type comparator [11], can perform the Analog-to-Digital (A/D) conversion in one clock cycle (like a full flash ADC). The main advantage of the modified flash ADC approach is the great reduction in the number of comparators. Therefore the device obtains a great power saving and size reduction.

To obtain 12-bit resolution, the pipeline ADC is designed to have 3 stages, each stage contributes 4-bit resolution.

3.5. System Controller

The system controller should make logical decisions based on the input signals to instruct the constituent components (including 4:1 MUX, SHC and 12-bit 3-stage pipeline ADC) to perform their functions properly at the correct instance. Figure 8 shows the timing diagram of the constituent components that are directed by the system controller (time not to scale). The designed pipeline ADC includes 3 consecutive stages, thus the total pipeline ADC conversion time includes the conversion time of the three stages. Besides, the MUX channel selection can be performed before the start conversion because the SHC will keep the data until a next 'start' signal applied.

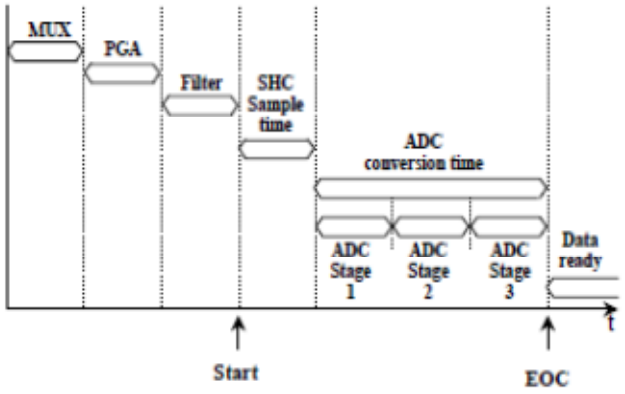

Fig. 8. DAQ system control signal timing diagram

III. sults

Two DAQ systems, using traditional 4-bit full flash ADC and the modified flash ADC topologies in a pipeline architecture, have been both implemented and simulated in Cadence. The performance of the two approaches are summarised in Table 1.

The layout of the designed DAQ chip employing the modified flash ADC to attain reduced power and complexity has been implemented and is illustrated in Fig. 9. The results of the layout simulation of the DAQ chip have been back annotated and analysed. Table 2 presents the simulation results of the layout DAQ chip.

IV. Conclus

A 12-bit, 4-channel fully CMOS DAQ chip has been presented. It operates at 1GHz master clock frequency and achieves a sampling speed of 125MS/s.

The DAQ system was implemented using both traditional flash ADC and modified flash ADC architectures. It can be seen that using the new modified flash approach greatly reduces the system power consumption. It dissipates only 64.9mW of power as compared to 97.2mW when traditional flash ADC was used.

Results indicate that a 33% power saving is obtained when the new modified flash ADC is used instead of a full flash ADC. This type of DAQ system is well suited for high-speed low-power applications, such as high performance wireless communication, where speed and power consumption are of main concern. It also benefits multi-channel applications, such as power fault analysis, where several channels can be assessed at high speed using only single PGA, anti-aliasing filter, SHC and ADC.

Table 1

Performance summary of the DAQ systems using traditional flash ADC and modified flash ADC

Device delay	Using traditional flash ADC	Using modified flash ADC
Total delay	8ns	8ns
Max data rate	125MS/s	125MS/s
Max master clock speed	1GHz	1GHz
Device power consumption @ 800MHz system master clock		
MUX power consumption	0.4mW	0.4mW
PGA power consumption	6.8mW	6.8mW
Filter power consumption	9.5mW	9.5mW
SHC power consumption	7.1mW	7.1mW
Pipeline ADC power consumption	72.9mW	40.6mW
Controller power consumption	0.5mW	0.5mW
Total Power consumption	97.2mW	64.9mW
Other Parameters		
DNL	±0.5 LSB	+0.6/-0.5 LSB
INL	±0.5 LSB	±0.5 LSB
Resolutions	12 bits	12 bits
Supply Voltage	2.5V	2.5V

Fig. 9. Layout implementation of the designed DAQ chip

Table 2

Simulation results of the layout DAQ chip

Description	12-bit DAQ chip (using modified flash ADC)
Power Consumption	77.1mW
Max master clock speed	917MHz
Area	3.52mm^2
Resolution	12 bits
Technology	0.18µm CMOS
Voltage Supply	2.5V

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TIME-INTERLEAVED MIXED-SIGNAL TEST CORE DIGITIZERS

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DOI: 10.36724/2664-066X-2021-7-3-27-30

ABSTRACT

System-on-Chip (SoC) is one of the main driving forces that have been reshaping the consumer electronics industry. The SoC alternative to conventional systems design is growing in popularity as the device packing densi escalates due to the evolution of semiconductor technology. Moreover, the decrease in semiconductor feature size is permitting the increase of clock frequencies and component operating speed. These advancements necessitate the integration of system components due to package parasitics and lengthy interconnect. Furthermore, SoC devices offer a cheaper and more compact solution to the consumer electronics industry.An integrated mixed-signal test core approach to SoC data acquisition is a valued alternate solution to many of the problems involving conventional test. One such test core data conversion architecture incorporates a sub-sampling algorithm known as the multipass method of digitization. This method occupies a very small silicon area in exchange for an increased data conversion time. Time-interleaved test core digitizers provide the capability to reduce test time, increase sampling frequency and increase signal bandwidth. As an implicit result of this compact circuit and multipass processing methodology, significant reductions in noise and spurious tones are observed.

KEYWORDS: *mixed-signal, analog-to-digital, digitizer, time-interleaving, test*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

I. Introduction

The amalgamation of digital, analog, and mixed- signal components into a single integrated circuit (IC) presents test engineers with tremendous difficulties. The current mixed-signal automated test equipment (ATE) solutions involve off chip stimulus and measurement through SoC package pins or IC probes. The tradeoffs between test development time, device test time, ATE requirements and SoC design constraints (e.g. I/O pads) is one of the greatest challenges facing the test engineering paradigm.

The integrated mixed-signal test core [1] provides an alternative to conventional test of mixed-signal ICs. This work proposes that the test apparatus be integrated within the mixed-signal SoC. Test requirements of mixed-signal circuits are extremely diverse. As such, the test core incorporates an arbitrary waveform generator (AWG) for signal stimulus and a digitizer to capture analog results.

The test-core solution boasts many advantages. By integrating the test equipment many interconnect and packaging problems are resolved, the number of test I/O pins is reduced, and parallel testing is facilitated. Another advantage is that the characterization and production testing can be performed by the same test core. In short, the test core approach offers the ability to improve product time-to-market and reduce cost as the constraints on development and test time are relaxed and the ATE requirements are moderated.

In order to reduce costly silicon area, a very small, mostly digital, digitizer architecture was developed to implement within the test core. One of the most significant tradeoffs of this compact digitizer design is an increase in test time. The digitization algorithm, known as the multipass method [2], is responsible for the time-intensive capture of analog information.

Time-interleaved data conversion is an attractive method to increase the sampling frequency of ADCs. Time-interleaved ADC systems implement multiple ADCs each sampled at alternate instants of time. Hence, for every additional time-interleaved ADC the sampling frequency may be increased proportionally. Furthermore, each ADC is clocked at its specified operating speed maintaining the performance characteristics of the individual ADC.

The disadvantage of the multiple-ADC time- interleaved architectures is the mismatch errors between ADCs. Each ADC will produce different DC offsets, gain errors, distortion and clock skews resulting in an increased noise and possible spurious tones. However, research has demonstrated that these errors can be compensated or corrected for through concurrent or post-processing techniques [3, 4]. Other research proposes a randomization sampling technique to reduce spurious tones [5].

The integrated mixed-signal test core can greatly benefit from time-interleaving whereby increasing the sampling frequency can imply a reduction in test time. Moreover, the addition of digitizers to the test core solution results in the integration of additional comparators. Furthermore, the multipass method of digitization implicitly offers the capability to reduce noise and remove spurious tones resulting from comparator mismatch.

The test core was implemented in a 0.18-µm CMOS process. Test results confirm the advantages of time-interleaving test cores. An outline of the paper is as follows: Section 2 reviews the design and operation of the test core digitizer. The time-interleaved test core is described in Section 3. Simulation and experimental results are revealed in Sections 4 and 5, respectively. Finally, Section 6 summarizes the proposed test system.

II. Mixed-Signal Test Core Digitizers

The integrated mixed-signal test core digitizer uses the multipass method of analog-to-digital conversion. This method operates on the premise that a periodic waveform of a known frequency is to be digitized. The frequency of the input signal is set by the coherency principle such that $F_T = MFS/N$, where F_T is the input waveform frequency, F_S is the sampling frequency, N is the number of samples per input waveform period and M is the number of input waveform periods to be captured within a unit test period (UTP). A UTP is the time it takes to collect N samples of the input waveform (i.e. $UTP = M/F_T = N/F_S$). For coherency, M and N should be integers, and for maximum information gathering, they should also be relatively prime to one another.

The multipass system, illustrated in Fig. 1, uses a 1-bit quantizer to compare 2^D-1 DC reference levels to all points on the periodic input waveform, where D is the number of bits that the converter can resolve. For each input waveform pass (or UTP), one reference level is established and compared to all N points of the test signal. The test signal waveform is reconstructed by summing all the digital outputs from each UTP that correspond to the same sampled instant on the waveform.

For Example, Fig. 2 illustrates the test signal and DC reference for a complete digitization cycle when D=3, M=1 and N=16. Within each UTP the test signal is sampled 16 times and compared with a single reference level. The digital result from each sample is stored in memory. The output from a complete conversion may be conceptually rearranged, as shown in Fig. 2b, to reveal the test signal waveform.

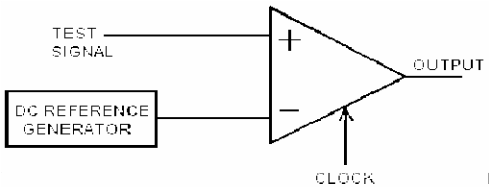
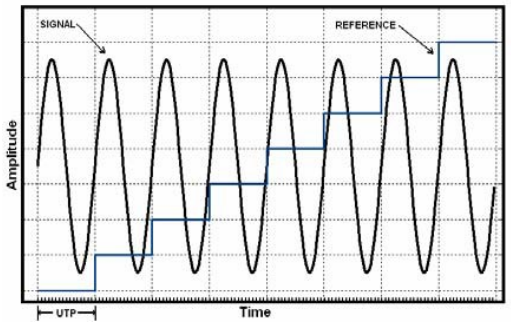
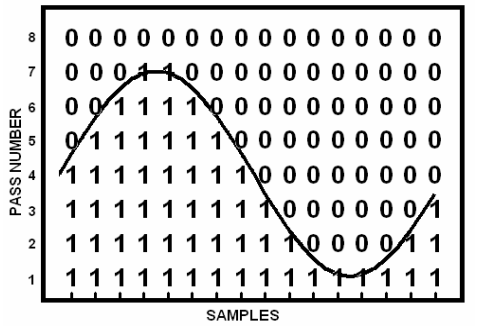


Fig. 1. Test Core Digitizer Architecture

The signal is reconstructed by summing the columns of Fig. 2b, as seen by the sinusoidal overlay. Alternatively, the output could be interpreted as a thermometer code.



(a)



(b

Fig. 2. 3-Bit Multipass Digitization Example (a) Input Test Signal and Reference; (b) Digital Recombination Process

At sampling clock periods smaller than the settling time of the comparator, a sub-sampling scheme would be employed within the multipass method, thus increasing the time to test. Time-interleaving multiple test core digitizers (i.e. comparators) can increase the effective sampling rate. By increasing the sampling frequency, sub-sampling would no longer be required.

III. Time-Interleaved Test Core Dig ers

The sampling frequency of an ADC is limited by circuit constraints and the tradeoffs between resolution and operating speed. Moreover, the input signal bandwidth of an ADC may be restricted by the maximum sampling frequency (i.e. Nyquist principle). Time-interleaved data conversion is an attractive method to increase the sampling frequency of ADCs. However, mismatch effects in these devices severely limit its performance by way of increased noise and spurious tones.

A time-interleaved mixed-signal test core system with five comparators is illustrated in Fig. 3. Each comparator will incorporate an input sample and hold stage and an output latch which are clocked by a phase generator. The comparators are stimulated by the same analog test signal and DC reference. Hence, the total design size only increases by the size of the additional four comparators. More importantly, the test time reduces by a factor of five.

IV. Simulation Resu

Using MATLAB the multipass method of digitization was simulated using the time-interleaved arrangement shown in Fig. 3.

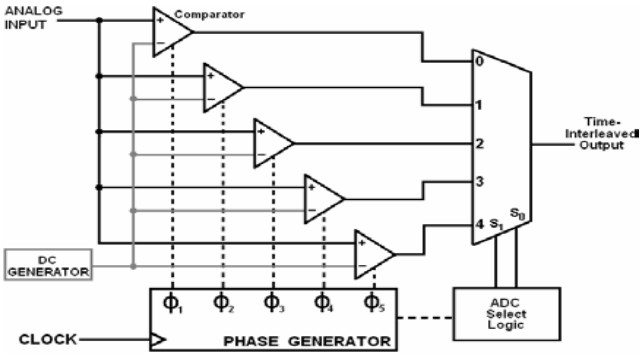
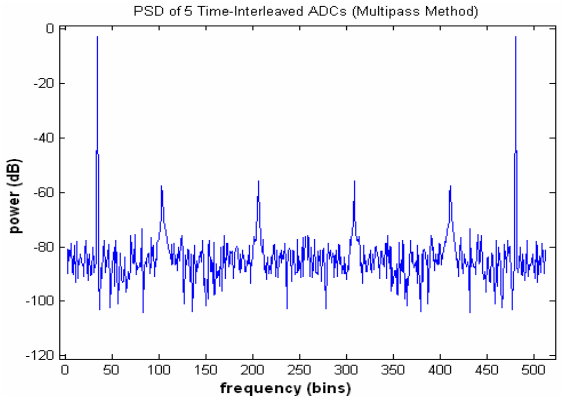


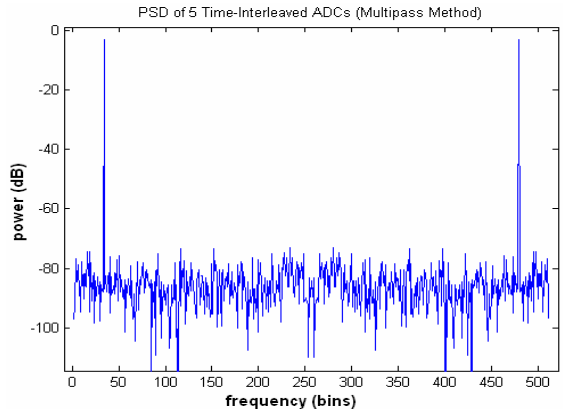
Fig. 3. Five Time-Interleaved Test Core Digitizers

Several sampling schemes were implemented to demonstrate the advantage of the test core.

The first sampling scenario, resulting in the power spectral density (PSD) shown in Fig. 4(a), involves reusing the same comparator to capture the same point in every pass of the multipass method. In this situation the mismatch between each comparator results in spurious tones. This situation is the typical result from any time-interleaved ADC system.



(a)



(b)

Fig. 4. Simulation Results Demonstrating the Multipass Benefit of Noise and Spurious Tone Suppression, (a) Time-Interleaved Digitization Mismatch Effects, (b) Multipass Method Suppressing Spurs

The second method of sampling consisted of rotating the comparators such that a different comparator, selected sequentially, is used to capture the same points in every pass.

Fig. 4(b) presents the PSD from this sampling method. It is clearly seen that the spurious tones are removed. In effect, the systematic mismatch errors have been evenly spread over the reconstructed waveform, thus contributing to the DC component. The distortion mismatch errors have been distributed over the entire signal bandwidth. The net difference between the two sampling conditions is a slightly better SNDR but a significantly improved SFDR. Most importantly, in conventional time-interleaved ADC systems, the second sampling algorithm is not possible.

V. Experimental Results

The time-interleaved test core digitizer, depicted in Fig. 3, was implemented in a 0.18-µm CMOS process. The microphotograph of the fabricated IC is shown in Fig. 5. The IC was tested using a Teradyne A567 ATE. Fig. 6(a) demonstrates the time-interleaved test core digitizer when each comparator is used to capture the same points through every pass of the multipass method. Fig. 6(b) results when alternating comparators are used to sample the same points from each pass.

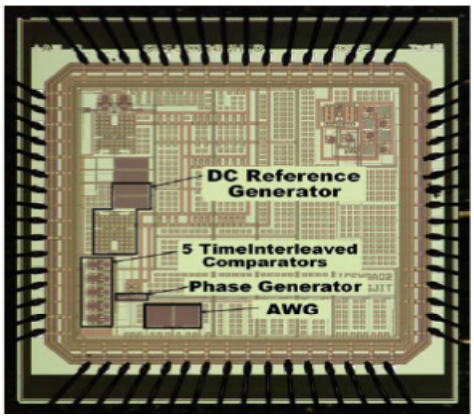


Fig. 5. Microphotograph of the Integrated Time- Interleaved Mixed-Signal Test Core in a 0.18-µm CMOS Process

Table 1 provides some of the numerical transition parameter results from each figure. It may be seen that SNR and SNDR are slightly better when the comparator usage is varied for each DC reference. However, the SFDR due to the mismatch induced spurs has increased 17 dB!

Table 1

Comparison of Figure 6 (a) and (b) Dynamic Performance Results

	Figure 6 (a)	Figure 6 (b)
SNR	48 dB	51 dB
SNDR	46 dB	48 dB
SFDR †	55 dB	72 dB

† comparing mismatch-induced spurs (not including harmonics)

A second experiment was performed to demonstrate that there is no performance degradation between a single digitizer and the time-interleaved counterpart. While sampling a 160 kHz test signal at 10 MHz a single test core digitizer assumed a SNDR of 48 dB. The five time-interleaved test core digitizer achieved a SNDR of 49 dB.

VI. onclusion

The mixed-signal test core digitizer is an attractive alternative to conventional test of high performance SoCs. This area efficient design suffers a lengthier test data conversion time. Time-interleaving can reduce test time at an area cost of additional comparators. It was demonstrated that no performance degradation is observed due to comparator mismatch.

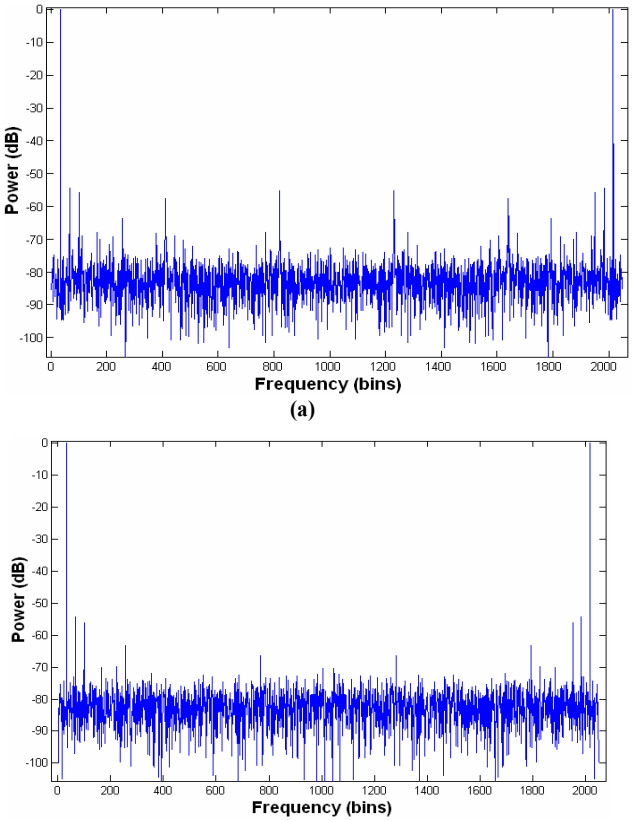


Fig. 6. Experimental Results Demonstrating the Multipass Benefit of Noise and Spurious Tone Suppression, (a) Time-Interleaved Digitization Mismatch Effects, (b) Multipass Method Suppressing Spurs

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A 19 MW, 12.5 B, 2.1 MS/S SINGLE-BIT ΔΣ ADC IN 0.18 μm DIGITAL CMOS PROCESS

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DOI: 10.36724/2664-066X-2021-7-3-31-35

ABSTRACT

The increasingly stringent requirements of today's communication systems and portable devices are imposing two challenges on the design of high-resolution, high-speed ADCs and delta-sigma modulators (ΔΣMs) in particular. The first is the extension of the input frequency range to include applications where the input bandwidth exceeds the 1 MHz range, while maintaining a feasible sampling frequency. The challenge in extending the operational speed of ΔΣMs is further rendered more complicated by the ever shrinking transistor dimension, and in turn, the supply voltage, hence the second challenge. To address those two challenges, the ΔΣMs presented in this paper targets a minimum of 12 bits in resolution at 2 MS/s Nyquist conversion rate, while using a single 1.8 V supply and minimum power dissipation.A switched-capacitor (SC) ΔΣ ADC integrated circuit (IC) with output rate slightly exceeding 2 MS/s was successfully implemented in a 1.8 V, 0.18 μm standard CMOS process. The IC consists of a fourth-order, multi-stage (2-1-1), single-bit modulator sampled at an oversampling rate of 50 MHz. Special effort has been made to reduce the power consumption of the modulator through careful system-level modeling and synthesis of circuit specifcations. Experimental results reveal a 77.6 dB dynamic range while consuming 18.8 mW of power, making it the lowest power dissipation for output rates in excess of 2 MS/s.

KEYWORDS: *digital CMOS process, portable devices, feasible sampling frequency.*

Article materials were presented at the 2nd IEEE International Conference on Circuits and Systems for Communications

1. Introduction

While many state-of-the-art lowpass ΔΣMs integrated circuits are published in the literature, some of which are presented in [1]-[5], they vary in their performance, output rate, power dissipation, technology, choice of architecture and sampling frequency, f_S. With this wide range of design criteria, it is unclear as to which modulator provides the best "overall" performance. While some modulators might have a superior resolution, the power dissipation could be very large too. It is therefore important that we make proper comparison using the most relevant metrics. It is those metrics discussed in Section 5, Modulator Comparison, that will reveal the superior performance of the experimental results of the circuit presented in this paper.

Following the introduction and the motivation behind this work, Section 2 of this paper presents a system-level description followed by the design of the main building blocks of the modulator in the third section. Experimental results demonstrating the functionality and performance of the ΔΣM are presented in Section 4, while performance comparison to other state-of-the-art modulators is presented in the Section 5. Concluding remarks are given in the last section of the paper.

2. SYSTEM-LEVEL DESIGN

In order to achieve good overall performance, it was important to minimize the power dissipation. In order to do so, the architecture had to be selected f rst. Then, it was essential to choose the minimum specif cations on each building block in the modulator that meet the target dynamic range. This was achieved through modeling the amplif er's bandwidth, slew rate, thermal noise, the comparator's offset, the input sampling network distortion and thermal noise contribution, all at the system-level. Once modeled, a set of design specif cations for the modulators's building blocks could be synthesized. With this modeling and synthesis, over-designing the modulators' building blocks is prevented which in turn keeps the power dissipation minimal. The details of the modeling and a new optimization and synthesis method that is computationally eff cient are presented elsewhere. Interested readers are referred to [6][7]. While the system-level design is one of the important keys in achieving a good resolution, the goal of this paper will be focused on the circuit implementation and the experimental results. The effectiveness of the synthesis method will be verif ed through the implementation of a fourth-order, cascade architecture consisting of three stages (2-1-1), all having single bit quantizers. With a minimum of 12 bits as a target resolution, an oversampling ratio, OSR, of24 is needed. With this OSR and an input bandwidth slightly exceeding 1 MHz, the corresponding sampling frequency, fs, is 50 MHz [5].

A summary of the non-idealities considered and their synthesized values are presented here and are shown in Table 1.

Table 1

Summary of synthesized versus implemented circuit specif cations

Block	Non-Ideality	Synthesized	Designed
OTA (C_L=1.5 pF)	DC Gain (dB)	72	100
	Gain-Bandwidth (MHz)	293	410
	Slew Rate (V/μs)	220	236/246
	Input Thermal Noise Density ($nV/\sqrt{Hz}$)	3.1	2.36
Comparator	Offset (mV)	60	-
Switch	$R_{max} = f(V_{in})$ (Ω)	540	119

3. SC CIRCUIT IMPLEMENTATION

The mapping of the previously synthesized block specif cations to a switched-capacitor implementation is presented in this section. In particular, the design of the operational transconductance amplif er (OTA) is presented in details followed by other blocks such as the comparator, the switches, the clock generator, the capacitors and the full circuit implementation.

3.1. OTA

A single-stage OTA was used due to its excellent frequency characteristics. A two-stage operational amplif er was avoided as it becomes power-hungry in low-voltage applications. The single-stage OTA was implemented using the folded-cascode topology with complementary differential pair at the input and n- and p as gain boosting stages at the output, as shown in Figure 1.

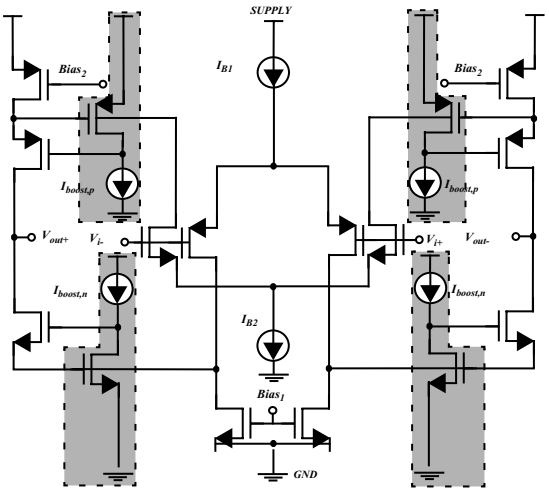

Fig. 1. OTA schematics with n- and p-gain boosting stages highlighted

The addition of the gain boosting results in an increase in the output impedance on the order of magnitude $g_m \cdot r_o$, which in turn results in an increased OTA DC gain.

On the other hand, the addition of the complementary differential pair at the input of the OTA has the advantages of increasing the bandwidth and providing a faster step response [8]. This is the result of increasing the effective transconductance, $g_{meffective,}$ which becomes the sum of both transconductances g_{mdiff} and $g_{mdiffcomp}$.

As a result, the DC gain and bandwidth are increased by a factor equal to $(g_{mdiffcomp} + g_{mdiff})/g_{mdiff}$. The addition of the complementary differential pairs allows also for a larger OTA input swing.

The above advantages happen at the expense of increased power consumption and increased parasitic capacitances, and if not designed properly could result in excessive high frequency performance degradation where the single-stage OTA behaves more like a multi-stage design.

In order to optimize the sizing and biasing of the transistors, small-signal analysis was performed. In [8] and [9], the small-signal analysis was detailed for gain-boosted telescopic amplifiers, and was used here as a guideline with the appropriate modifications for the OTA topology under considerations. Detailed pole-zero map analysis was carried out in order to carefully size the biasing current and the transistors in the gain boosting stages and the complementary differential pairs to increase the OTA DC gain and bandwidth without degrading its frequency behavior. The effect of sizing both gain boosting stages (for given currents in the different branches of the OTA and given saturation voltages) was simulated in Matlab with transient and AC analysis performed. Corresponding pole-zero maps were also plotted to observe the locations of the poles and zeros as the current in the gain boosting stages was varied.

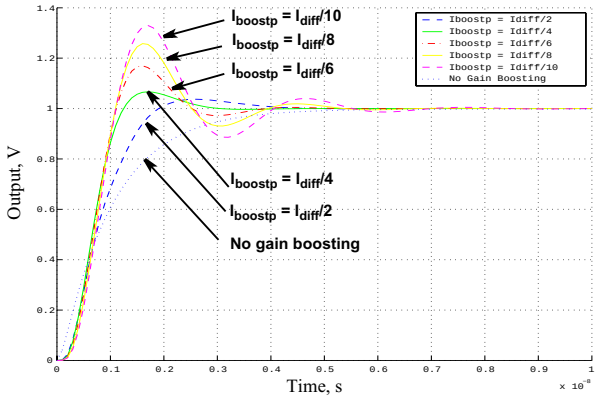

Fig. 2. Step response of the OTA as a function of the p-stage gain boosting current

Figure 3 shows a plot of the poles and zeros as modeled in Matlab, for a boosting current in the p-stage1, *Iboost,p* being equal to 1/4th the current in the main differential pair, IB ($I_{boost,n}$ was fixed to a scaled version of $I_{boost,p}$. The discussion, while referring to $I_{boost,p}$ hold equally for $I_{boost,n}$).

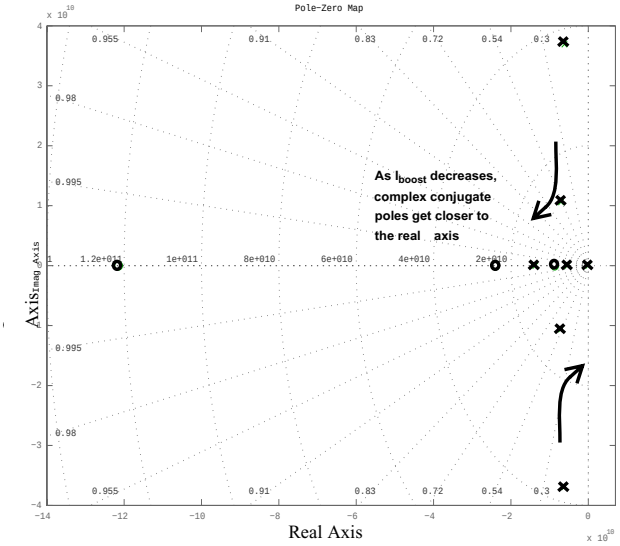

Fig. 3. OTA pole-zero map for $I_{boost,p} = I_{diff}/4$

As the current in the gain-boosting stage decreases, the complex conjugate pairs start to get closer to the real axis until eventually the two complex conjugate poles become real which results in reduced phase margin, ringing in the step response and therefore frequency response degradation of the OTA (Figure 2). Increasing the gain boosting current will, on the other hand, increase the power dissipation.

A tolerable ringing that does not degrade the overall performance of the modulator dictates the choice of the current in the gain boosting stages. A SC common-mode feedback (CMFB) was used in all the above analysis and was chosen due to its low power dissipation. The switches in the SC-CMFB were implemented using transmission gates.

Based on the above analysis, proper system-level modeling allows for careful transistor sizing and biasing choices. With that, low power dissipation could be achieved while still using a single-stage amplifier and while meeting the stringent requirements imposed on the OTA using a single 1.8 V supply and that were synthesized at the system level and summarized in Table 1.

The OTA output swing is though limited to 0.5 V measured differentially. Implications of this limited swing will be discussed further when experimental results are presented.

3.2. Comparator

A CMOS dynamic comparator, with core shown in Figure 4, and a clocked RS latch were used to implement the single-bit quantizer. No pre-amplification stage is used due to the comparator's relaxed offset requirements. To account for hysteresis and the effects of mismatches due to process variations, the comparator was designed to achieve a resolution equivalent to 11 bits, capable therefore of resolving a differential signal of ~880 μV in the current technology.

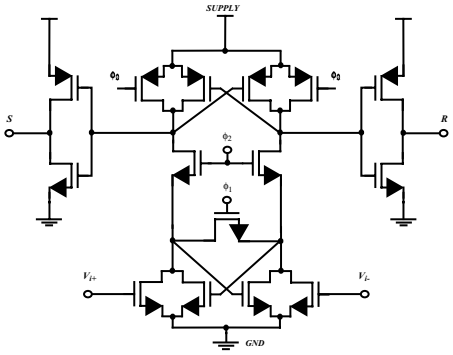

Fig. 4. Comparator core schematics

3.3. Other Blocks

a) Switches

Most designs implemented in deep submicron technologies with minimum feature length less than 0.35 µm and with a supply voltage lower than 3.3 V resort to bootstrapping for the switches. The current paper shows the possibility of implementing the modulators's switches with simple transmission gates. The advantages of using transmission gates is the simplicity of the circuit, and the power and area savings. With proper transmission gate sizing, it is argued that transmission gates suff ce if they are sized to limit their distortion. The experimental results will back up this claim. A design implemented in 0.25 µm technology using a single 2.5 V supply further backs up the current claim. The design achieved 15 bits in dynamic range with simple transmission gates [6]. The switches were implemented using regular transmission gates. The NMOS and PMOS transistors were sized appropriately in order to keep their on-resistance low enough to limit the harmonic distortion [6]. The peak on-resistance of the designed transmission gate was limited to 119 Ω. An on-chip four-phase non-overlapping clock generator was used to clock the switches. Delayed versions of the clocks (together with fully differential implementation) were used to minimize charge injection.

b) Capacitors

While absolute capacitor values are not critical in switched-capacitor designs, matching is of utmost importance since capacitor ratio is primarily responsible for pole/zero placement in the system. Shift of these poles/zeros result in different NTFs and STFs which could possibly result in an increased noise in the band of interest. In some cases, instability might even occur, but is unlikely to happen if the system was designed to be stable under the worst-case variation in capacitor values. In order to achieve best matching, all capacitors were built from a unit-size metal-metal capacitor equal to 125 fF with common centroid techniques adopted. Metal layers 3 through 6 were used, while metal layers 1 and 2 were avoided due to their increased parasitic capacitances with respect to the substrate. Top-metal layers forming the top plate of the capacitor were used to connect to sensitive nodes (such as op amp inputs) due to their lower parasitic capacitances, while lower-metal layers constituting the lower plate of the capacitor were used to connect to less sensitive nodes (such as op amp output nodes). Additional dummy capacitors left unconnected were included around all capacitor arrays to minimize etching effects.

3.4. Full Circuit Implementation

The synthesized block specif cations were mapped into a fully differential SC circuit with capacitor values and modulators' analog coeff cients (given by the capacitor ratios) shown in Figure 5. The digital error cancellation block used to convert the outputs of the three stages into a single fourth-order noise shaped signal was implemented in software with digital coeff cients directly deduced from the analog coeff cients with relationships between the analog/digital coeff cients found in [5]. The SC circuit was then mapped into the IC shown in Figure 6, using a 0.18 µm, single-poly, 6-metal digital CMOS process.

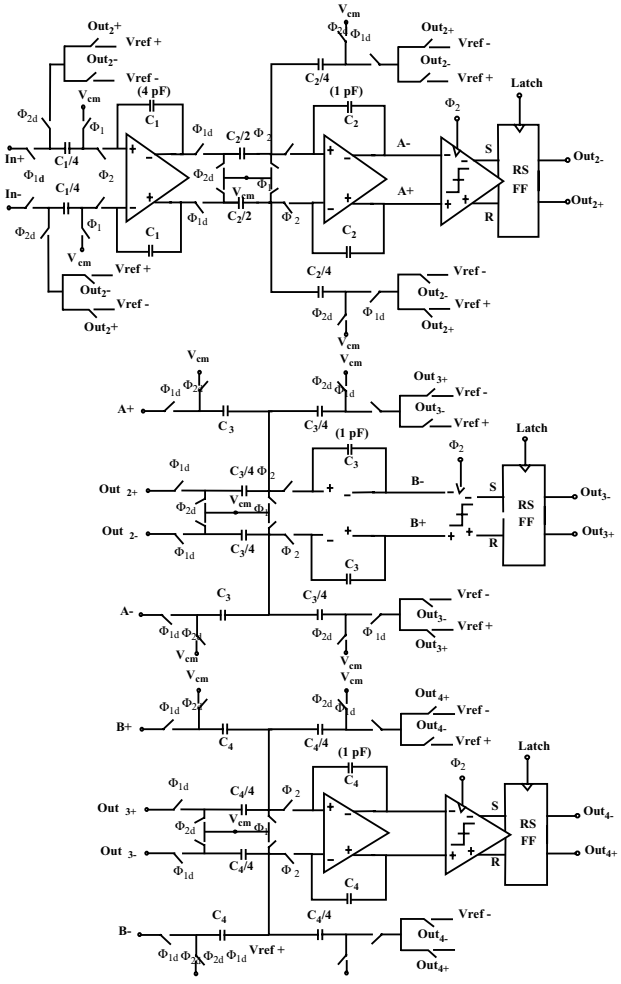

Fig. 5. Three-stage (2-1-1) SC-implementation

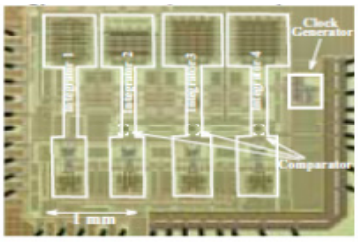

Fig. 6. IC microphotograph

4. EXPERIMENTAL RESULTS

In order to evaluate the performance of the IC, a custom-made four-layer PCB was designed. Separation of analog and digital planes, de-coupling capacitors and voltage regulation for the supply voltage lines were included. The differential input was generated using a Teradyne A567 mixed-signal tester and the clock using a high-quality Hewlett Packard pulse generator model number 81130A. The measured dynamic range (Figure 7) was 12.6 bits of dynamic range where dynamic range is def ned as the difference between the two input levels for which SNDR ≥ 0 dB. The distortion is higher than predicted; the measured total harmonic distortion was 62 dB for a 0.6 V p-p sine wave. This could be explained by the fact that the DAC reference voltages, Vref+ and Vref- were set to full scale (1.8 V and 0 V respectively). The input of the OTA was designed to handle a large swing. The output, however, had a swing that was limited to ~ 0.5 V. On the other hand, shrinking Vref+ and Vref-from full scale to 1.3 V and 0.5 V, respectively, resulted in a decrease in the total harmonic distortion at the expense of an earlier saturation in the input level. This in turn caused a decrease in the peak SNR. Table 2 summarizes the IC measured specif cations.

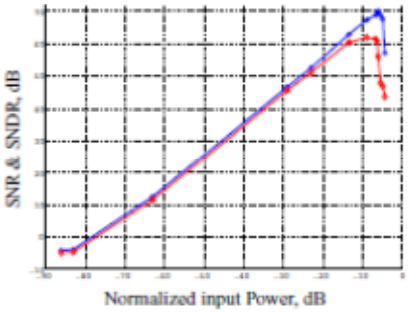

Fig. 7. Measured dynamic range

Table 2

Summary of measured specif cations

Technology / Supply	0.18 µm CMOS / 1.8 V
Power Dissipation	18.8 mW
(V_{ref+}, V_{ref-}) / Input Range	(1.8 V, 0 V) / 1.5 V_{p-p}
f_s, *OSR*, Output Nyquist Rate	50 MHz, 24, ~2 MS/s
DR*, Peak *SNR*, Peak *SNDR	77.6 dB, 70 dB, 62 dB

5. MODULATOR COMPARISON

To evaluate the performance of the modulator with experimental results presented in the previous section in the context of some state-of-the-art lowpass ΔΣMs integrated circuits published in the literature, a f gure of merit, FM is introduced in [5] and is def ned as $FM = P / (2^b \cdot BW)$, where b is the bit-resolution, BW is the output rate, and P is the power dissipation. This f gure of merit could be used to classify the performance of the modulators where a lower FM corresponds to a more performing modulator. A plot of FM as a function of supply voltage is shown in Figure 8.

The designs shown in Figure 8 were chosen among many state-of-the-art implemented in different technologies and using a variety of supply voltages, due to their lowest achieved f gure of merit FM.

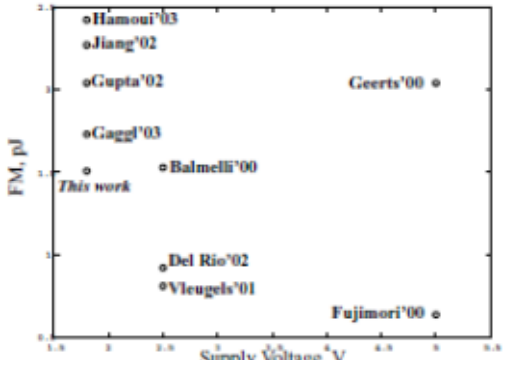

Fig. 8. Performance comparison of some published state-of-the-art ΔΣMs

With this criteria, the modulator implemented ranks well among the best modulators published to date. In terms of supply voltage used, the modulator uses the lowest supply voltage for the modulators' analog core and dissipate the lowest power among the output rates exceeding 2 MS/s.

6. CONCLUSIONS

We have presented the implementation and experimental results of a single-bit ΔΣ ADC in 0.18 µm, single-poly, 6-metal CMOS technology. Minimum power dissipation was achieved through careful system-level modeling and synthesis of circuit specif cations which proved eff cient. A widely adopted f gure of merit reveals the superiority of the achieved performance of the modulator, placing it among the top published to date according to the open literature. Using a single 1.8 V supply, the modulator consumes the lowest power dissipation among the modulators of its class where the output rate exceeds 2 MS/s.

ACKNOWLEDGMENTS

This work was supported by Micronet, a Canadian network of centres of excellence dealing with microelectronic devices, circuits and systems and the Canadian Microelectronics Corporation.

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ITU REVIEWS 2021
(PART 2. THEMATIC BACKGROUNDERS)

The International Telecommunication Union (ITU) is the United Nations specialized agency for information and communication technologies (ICTs), driving innovation in ICTs together with 193 Member States and a membership of over 900 companies, universities, and international and regional organizations. Established over 150 years ago in 1865, ITU is the intergovernmental body responsible for coordinating the shared global use of the radio spectrum, promoting international cooperation in assigning satellite orbits, improving communication infrastructure in the developing world, and establishing the worldwide standards that foster seamless interconnection of a vast range of communications systems. For more information, visit www.itu.int.

ACCESSIBILITY TO ICTS

OVERVIEW

• Given the growing proliferation of devices in our lives, it is vital that persons with disabilities (PwDs) or rare diseases can fully access Information and Communication Technologies (ICTs) and the opportunities they provide in their own right. Digital accessibility is key to ensuring respect for everyone's right to be able to participate in an interconnected world, as it enables digital inclusion and inclusive discourse for all people - regardless of age, gender, ability, or location.

• Common examples of accessibility features include: voice-to-text conversion (captioning), automated sub-titles and sign language for the deaf or hard of hearing and expandable font sizes.

• ICTs also offer hope for improving quality of life and social inclusion for Persons with Disabilities now and in the future, including: brain-to-machine interfaces, self-directed mobility aids and autonomous cars.

• The World Bank estimates that one billion people suffer from some sort of disability. By 2030, the number of senior citizens aged 60 and above who face age-related disabilities is expected to reach 1.4 billion, rising to 2.1 billion by 2050 [1]. Moreover, 1.1 billion youth are in danger of experiencing some form of hearing loss due to their unsafe listening habits[2]. Given these figures, within thirty years, half of the world's population could be affected by some form of disability.

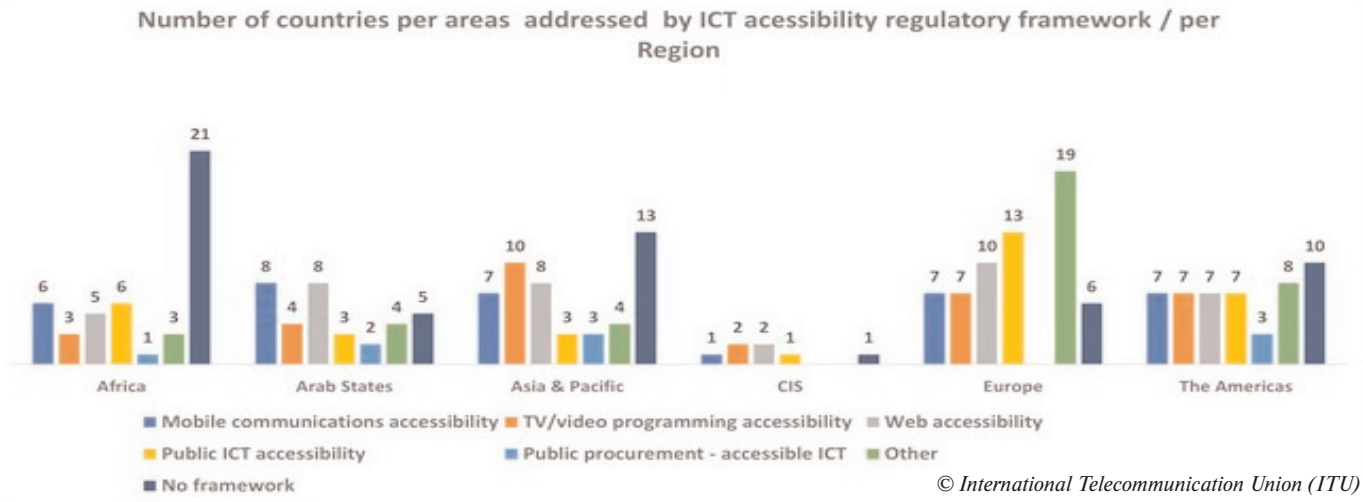
• Persons with Disabilities can suffer from a wide range of conditions, from congenital conditions to specialized needs brought about by rare diseases, injuries inflicted though accident or illness, impairments to sensory or perception loss or age-related illnesses. Private companies may not voluntarily include accessibility features in their products and services, so there is a strong role for Government policy to ensure accessibility of services, as well as technical standards to ensure accessibility is taken into account in the design of technological products and services.

CHALLENGES

An estimated one billion persons live with disabilities, of which 80% live in developing nations, where infirmity and disabilities are real drivers of exclusion and poverty. The WHO estimates that, globally, the number of people with visual impairments is around 285 million, of whom 39 million are blind, with people over 50 years old accounting for 82% of all blind people [3]. WHO also estimates there are 466 million persons with disabling hearing loss, some 6.1% of the global population [4].

Article 9 of the UN Convention on the Rights of Persons with Disabilities (PwDs) defines ICT accessibility as an integral part of accessibility rights, on a par with transport and the physical environment[5]. A multi-stakeholder coalition of partners including ITU and the UN Broadband Commission for Sustainable Development has stated that "no one should be excluded from using mobile phones, the Internet, televisions, computers, electronic kiosks and their myriad of applications and services including in education, political life, and cultural activities or for e-government or e-health to cite a few examples. Being excluded from ICT-enabled applications implies being shut out from the information society, as well as from accessing essential public services and the opportunity of living an independent life" [6].

Furthermore, digital accessibility is recognized as a key priority in various global commitments related to inclusiveness, such as: the Convention on the Rights of Persons with Disabilities (CRPD), the 2030 Agenda, the Sustainable Development Goals (SDGs) and the UN Disability Inclusion Strategy.



SOLUTIONS

Making ICTs and ICT services accessible is not just a human rights issue or a question of justice and equality of access to communications, information, and opportunities for all. ICTs can make a very real difference to the quality of life of people living with difficult or debilitating conditions or disabilities. Examples include:

• Voice-to-text conversion for the hard-of-hearing.

• Expandable font sizes or text-to-voice conversion for people with deteriorating or failing and degraded eyesight.

• Warning, space, and motion sensors for people with poor or limited sight.

• Digital libraries for deaf persons or hard of hearing.

• Global Positioning System (GPS) navigation for people with location amnesia.

• Photo albums or voice recordings for people with amnesia, dementia, or short-term memory loss, to remind them of their past and the identity of friends and relatives.

• The prospect of independent mobility via autonomous and self-driving cars for blind persons or people with poor eyesight.

• Machines to produce speech for people with e.g. motor neurone disease, who are no longer able to speak.

Some neurological problems that people experience-including some types of memory loss, depression, blindness, and seizures, to name a few-are the result of erratic or absent electrical signals in parts of the brain. Various research projects are underway on brain-machine interfaces.

ITU'S CONTRIBUTION

The ITU Plenipotentiary Conference 2018 renewed ITU's mandate in the area of ICT accessibility, inITU Resolution 175 (Rev. 2018) on "Telecommunication/ICT accessibility for persons with disabilities and persons with specific needs". It also approved the Connect 2030 Agenda, which sets out the vision, goals and targets that ITU and its Member States have committed to achieve by 2023. All three ITU Sectors have approved specific resolutions on accessibility at their respective Conferences[7].

ITU's Member States are fully committed to advancing ICT accessibility implementation in their countries and regions. The Connect 2030 Agenda includes a bold target directed at cultivating government commitment to make the ICT sector inclusive of persons with disabilities and specific needs. Target 2.9: Enabling environments ensuring accessible telecommunication/ICT for persons with disabilities should be established in all countries by 2023.

ITU has developed a series of resources to support ITU Member States in creating enabling environments ensuring accessible telecommunication/ICT for PwDs, and in building inclusive digital societies in their countries and regions. According to ITU's latest data, by 2019, 84 countries had established a regulatory framework to ensure ICT accessibility for persons with disabilities (Figure below). Regulatory frameworks can include accessibility requirements for: mobile communications; web accessibility; public procurement of accessible ICT; TV or video programming; and public ICT accessibility, as well as other areas.

ITU's Standardization Sector (ITU-T) develops international standards known as ITU-T Recommendations. Its work on accessibility started in the early 1990s with ITU-T V.18 text telephone. Since then, a number of ITU standards on accessibility have been developed within ITU-T SG16, Question 26/16 on accessibility and Question 24/16 on human factors and cooperated with advocacy organizations (such as the G3ict, WFD and RNIB), in addition to other technical groups such as ITU-T, D, R Study Groups and ISO/IEC JTC1 SC35. A sample of which is found in the ITU-T Accessibility and Standardization.

Recently approved ITU-T Recommendations on accessibility include:

• ITU-T F.791 (08/2018) provides accessibility terminology and terms with definitions harmonized with UN CRPD definitions.

• ITU-T F.921 (08/2018) describes how audio-based network navigation systems can be designed to ensure that they are inclusive and meet the needs of persons with visual impairments.

• ITU-T F.930 (03/2018) describes functional description of four common types of relay services in use today: text relay; video relay; captioned telephone service relay; speech-to-speech relay.

• ITU-T H.702 (11/2015) defines the basic functions of accessibility services on IPTV.

• H.871(07/2019) provides characteristics of Personal Sound Amplifiers and suggests ways of informing consumers about the potential unacceptable noise levels when using these devices for prolonged periods of time.

• ITU-T Y.4204 (02/19) (ITU-T SG20) provides accessibility requirements for the Internet of Things (IoT) applications and services.

ITU-T also produces various Technical Papers on accessibility:

• FSTP-ACC-RCS (2018) provides introduction to remote captioning services, with background, technical, security and quality aspects.

• FSTP-ACC-RemPart (2015) provides guidelines to ensure that remote participation in meetings is accessible for persons with disabilities.

• FSTP-TACL (2006) provides checklist to ensure accessibility of specified services and features from the beginning of standards development process.

ITU's Development Sector (ITU-D) work in ICT accessibility supports the advancement of the global disability-inclusive agenda and the development of inc lusive digital communities. ITU-D helps raise awareness, build capacity and provide policy and strategy advice to ITU members. ITU-D has helped countries by implementing regional initiatives and activities linked to ICT accessibility in the Africa, Americas, Arab, Asia and Pacific European and CIS regions, through direct assistance to countries, development and provision of relevant guidelines, development and delivery of on-line and face-to-face trainings, toolkits, and reports, and by facilitating joint working platforms such as Study Group and regional "Accessible-ICT for ALL" knowledge development forums enabling stakeholders to share good practices and engaging in national and regional digital accessibility implementation. Finally, ITU-D is supporting members' efforts in mainstreaming digital accessibility to ensure the full and effective participation of everyone in the digital economy by developing and making available a series of useful resources.

AFFORDABILITY

OVERVIEW

The price of telecommunication and Internet services is regularly cited as one of major barriers to Internet access and usage. Monitoring prices is very difficult, as prices depend on: type of service (fixed versus mobile); bundling of different services; different operators (within the same market); data, voice and text allowances; and whether national or international comparisons are made.

There is evidence to suggest that affordability or the ability of individuals or households to pay for telecom services relative to their disposable income is one of the main barriers that affect consumer consumption of Internet services. Affordability depends not only on both price and income, but also on other, competing spending choices available.

Globally, prices for voice and data services have been falling over the last decade, in line with growing competition and strong increases in subscriber rates and usage.

ITU is the official source for global ICT data and statistics, including ICT price data. ITU has the responsibility for collection and reporting of global and national official telecommunication statistics as well as statistics for ICT household access and individual ICT use within the UN system. ITU works with other international organizations (e.g. the World Bank and OECD) to ensure the accuracy and international comparability of these data. ITU was a founding member of the Partnership on Measuring ICT for Development.

ITU monitors price data from ITU Member States via an annual survey, which are disseminated in the World Telecommunication/ICT Indicators Database and the ITU Yearbook of Statistics.

ITU also tracks the Connect 2030 Agenda, a set of indicators agreed by ITU membership, which includes affordability indicators and targets.

DEFINING PRICE VERSUS AFFORDABILITY

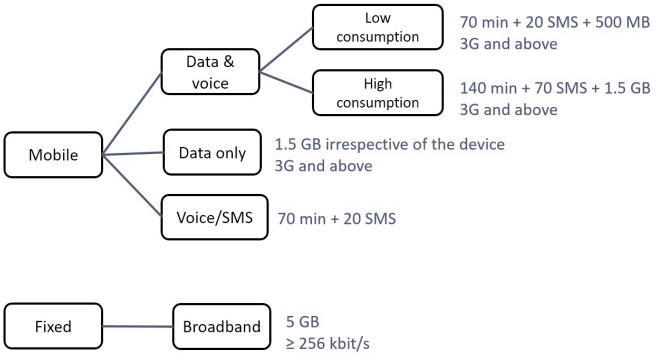
Defining the 'affordability' of telecom services can be very hard. This question can be answered statistically in different ways, depending on whether we examine:

- Direct comparisons between different operators in a single country or over time. Prices can vary due to: contract length; volume of minutes; texts and data allowances; and whether a handset is included.
- International comparisons: may require adjustments for exchange rates and purchasing power parity between different countries.

Standardized price baskets can be used to compare prices between operators and/or countries. Prices significantly influence the profitability of mobile operators, and their ability to survive, upgrade and reinvest in networks. Prices for initial service launches may be high ('premium pricing'), but usually fall as services are rolled out across larger subscriber bases (sometimes due to 'economies of scale' or 'predatory pricing'), sometimes resulting in lower prices for larger operators, with larger subscriber bases.

The 'price' of telecom/ICT services is often cited as a barrier to using telecom services, but there is evidence that what really matters is the 'affordability' or ease of purchasing a service, relative to consumer income. Prices can be expressed as a percentage of Gross National Income (GNI) per capita to show prices relative to the size of the economy of each country, thus pointing to the affordability of each ICT service at country level. Such national averages may not indicate that ICT services are affordable for poorer social classes, or any particular household or individual, but they still give insights into whether telecom services are affordable.

ITU has defined a number of price baskets:



Baskets provide a helpful standard benchmark for comparisons, but they have some drawbacks: there are many other packages available to consumers; they may not take account of the evolving consumer behavior over time; and they use a 'weighted average' price, irrespective of number of subscribers that use it.

For affordability, ITU monitors countries where low-consumption data and telecom services are affordable. There is still a small number of countries where data and telecom services are relatively unaffordable, costing above 10% of GNI per capita.

CHALLENGES

In 2018, the ITU/UNESCO Broadband Commission for Sustainable Development set out a target for 2025 that entry-level broadband services should be made affordable in developing countries, defined as <2% of monthly GNI per capita.

The lack of internationally comparable data makes it hard to assess the impacts of price bundling on consumer welfare, competition, and universal broadband access. Comparable data is needed, to enable regulators and consumers to compare prices and identify trends. ITU works closely with other regional and international bodies (including the UN, Eurostat, OECD and the Partnership on Measuring ICT for Development and country experts) on developing international definitions, standards and methodologies for telecommunication/ICT data.

The telecom/ICT sector is very complex, with many converged services. Historically, prices used to be paid and settled on the basis of per minute charges or tariffs. Today, however, many operators have moved to Internet Protocol (IP)-based networks and now price their communication services on a 'flat-rate' basis, for a certain amount of data. This relates to the consumption of services (e.g. movies, online games) for large amounts of data.

For mobile services, prices vary hugely between a pre-paid or basic entry package and more sophisticated packages. Prices may also vary 'on-net' and 'off-net'.

It can be difficult for consumers to compare the prices for different packages for even a single operator, at any point in time, with the ultimate price often depending on usage patterns among consumers (e.g. many operators offer free calls to 'favorite contacts'/friends & family and/or multiple phones linked with one household.

OPPORTUNITIES

Falling prices have been linked to increased subscription rates and greater usage of ICT services. Different stakeholders have a different role to play. Telecom operators have a vital role in defining, revising and pricing telecom packages for consumers – in terms of monthly subscription prices or prices per traffic. Historically, there is strong evidence to suggest that prices in mobile markets generally fell, following the introduction of strong and effective competition with alternative mobile operators.

ICT regulators often set reference interconnection offers, setting recommended or ceiling interconnection prices between operators (for example, this is what the Nepalese regulator has just done[i]). They often also set national benchmark prices and monitor markets through regular market surveys, to try and define, and ensure 'fair' and affordable prices for consumers, against fair returns for operators, so they can continue to invest and upgrade mobile networks.

Governments (Ministries and regulators) can also play a strong advocacy role, by signaling the importance of advanced 4G and 5G infrastructure at the national level (e.g. through a 5G Action Plan, Digital Agenda or other statement of policy). They can also convene dialogues and national consultations to define national priorities for the rollout of advanced digital infrastructure among different stakeholders.

ITU'S ROLE

ITU holds various responsibilities for data and statistics in the international system. At the 2014 Plenipotentiary Conference in Busan, Rep. of Korea, ITU membership agreed on the Connect 2020 Agenda, revised at the 2018 Plenipotentiary Conference to the Connect 2030 Agenda, containing various targets, to monitor progress towards a set of key indicators.

ITU has the reporting responsibility for formal collection and reporting of global and national official data and statistics for telecommunication/ICT within the UN system, and provides these data to international organizations (e.g. World Bank) and outside (e.g. the World Economic Forum, Internet World Stats and Statista).

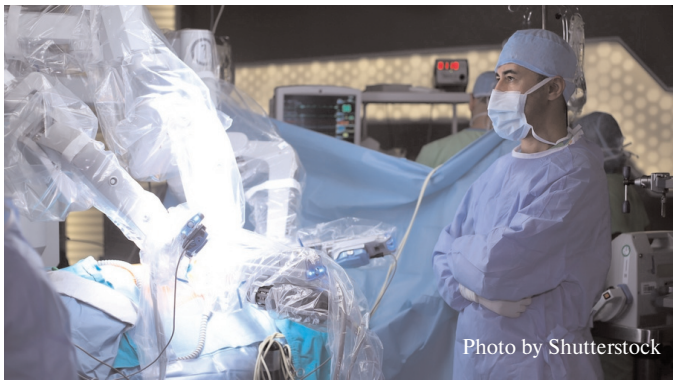
ITU carries out annual collections of: (1) telecommunication/ICT data from national telecommunication/ICT ministries and regulatory authorities on fixed-telephones, mobile-cellular services, Internet/broadband subscriptions, traffic, prices, revenues and investment; and (2) household ICT data, covering access to ICTs by households and use of ICTs by individuals, generally from national statistical offices (NSOs).

ITU-T Study Group 3 is responsible for "tariff and accounting principles including related telecommunication economic and policy issues" and fosters collaboration among ITU members in the interests of establishing telecom rates as fair and as low as possible.

ITU is the custodian of a number of SDG indicators (4.4.1, 5.b.1, 9.c.1, 17.6.2 and 17.8.1) and responsible for tracking them at the international level. These do not directly include price, but recognize the need for affordable Internet access.

ITU regularly hosts the "World Telecommunication/ICT Indicators Symposium" (WTIS) to discuss the latest key issues in the field of ICT statistics.

ARTIFICIAL INTELLIGENCE FOR GOOD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OVERVIEW

Artificial Intelligence (AI) comprises a rich set of methods and disciplines, including vision, perception, speech and dialogue, decisions and planning, problem solving, robotics and other applications that enable self-learning. AI is best viewed as a set of technologies and techniques used to complement traditional human attributes, such as intelligence, analytical ability and other capabilities.

ITU is engaged in a body of work about how AI can influence telecommunication and radiocommunication networks, as well as the broader information and communication technology (ICT) environment.

A robust enabling environment is necessary for driving innovation and trusted use of AI technologies. Development of policy must take into account the needs of specific user groups to avoid discrimination and ensure that everyone can experience the benefits of AI (including poorer communities, children, persons with disabilities and indigenous peoples).

Artificial Intelligence (AI) comprises a set of widely different technologies, which can be broadly defined and grouped together as 'self-learning, adaptive systems'. There are various approaches to defining AI:

In terms of technologies, techniques and/or approaches (e.g., a neural network approach to machine translation);

In terms of purpose (facial recognition, image recognition). In terms of functions (e.g., the ability to understand language, recognize pictures, solve problems, and learn, according to the Cambridge Dictionary). In terms of agents or machines or algorithms (e.g., robots, self-driving cars).

AI comprises a rich set of methods and disciplines, including vision, perception, speech and dialogue, decisions and planning, problem-solving, robotics and other applications that enable self-learning. AI is best viewed as a set of technologies and techniques used to complement traditional human attributes, such as intelligence, analytical ability and other capabilities. AI, Machine Learning (ML) and modern data techniques have been greatly enabled by recent advances in computer processing, power and speed, and advances in AI depend in turn on advances in data techniques.

OPPORTUNITIES

Across many sectors, AI offers advantages of new and innovative services, and the potential to improve scale, speed and accuracy. AI extends and combines many of these advantages with insights from statistics and big data. Based on trend analysis, AI helps move business and policy models and regulatory approaches from descriptive analysis and trendspotting to more sensitive, proactive predictive and evidence-based models and approaches. For example, AI is being used to spot patterns in health vulnerabilities and insurance risks, among many other applications.

The use of AI tools and techniques is driving new opportunities across many diverse domains. AI and other algorithms are used extensively in online search, entertainment, social media, self-driving cars, visual recognition, translation tools, smart assistants/speakers, voice-to-text and many other applications.?

CHALLENGES

Policy and regulatory frameworks for AI remain at an initial, formative stage. Key policy questions that have arisen relate to:

• Use, accuracy and methods used by AI tools, including in relation to humans, including the development of bias in machine learning models and the data used to train them;

• Accountability and responsibility accompanying the use of AI models;

• Purposes for which they are used as well as datasets used to train them, and the methods used to collect (or 'scrape') data.

Major questions arise in relation to the quality and representativeness of the datasets that have been used to train AI. Researchers are also working to improve the accuracy of software tools and algorithms, amid concerns they magnify racial and socioeconomic biases. For example, while the COVID-19 pandemic has, in many countries, disproportionately affected minorities, AI-based prediction models may not always include other relevant health disparities and thus may not always correctly assess risks for each person or group.

Data ownership has emerged as a major issue. Data must be continually aggregated to help keep every model valid, accurate and effective in predicting outcomes. There is an increasing proliferation of deep fakes (e.g. convincing programmed videos of high-profile personalities saying or doing things the video creator has requested) and other AI-generated materials. Indeed, deep fake technologies have been used to generate misleading videos in the mainstream media, as well as to animate photos of long-dead celebrities. Aside from crucial ethical questions about use and accuracy, who owns the copyright to these “new" works?

AI has extraordinary potential to act as a force for good. However, considerable challenges persist:

• Fundamental trust and the transparency of models: It is frequently unclear how deep learning models arrive at their conclusion and the models may be opaque and not very transparent. Depending on the purpose, although researchers want AI to make accurate predictions, some researchers may still prefer simple yet explainable AI models to more accurate, but more opaque models. Some people are willing to 'trust' machines with complex systems and tough decisions, while others may fundamentally prefer to retain some degree of human involvement.

• Bias: While AI can be used for extremely useful purposes, it can also inadvertently generate poor or inappropriate purposes or unintended outcomes. There is growing concern about issues of racial, disability and gender bias in AI and machine learning algorithms, and their wider impact on society at large. The accuracy of an AI ML model depends on the quality and the amount of data that an AI model is trained on. In real life, data is often poorly labelled. Standardization of data sets is needed. Data are also often biased. Training courses on the ethical applications of AI are needed, and not just for computer engineering students.

• Data availability and ownership: Getting data is very difficult. Best practices need to be defined under which circumstances data can be made available and to whom, whilst respecting ownership and explicit promises of confidentiality for certain types of data.

• Data privacy and security: Security breaches due to cyber-attacks can have horrific consequences. Techniques such as federated learning can reduce the risks by enabling AI models to be trained across devices that hold data locally, without exchanging them, while privacy-preserving technologies help ensure personal data protection.

• Limited know-how: AI can tackle many problems, but there is only a limited pool of experts who know how to apply AI ethically. Many researchers point to the need to involve sociologists and policy-makers in discussions, rather than assume that AI designed by a narrow pool of 'technologists', computer engineers and data scientists will be used ethically. Education is key to learn about the responsible use of AI.

• Equitable uses of AI: AI research is computationally intensive. Unequal access to computing power and to data deepens the divide between a few companies and elite universities which do have resources, and the rest of the world which does not.

THE POTENTIAL OF AI TO BE USED FOR GOOD

AI has many important applications to help accelerate progress towards achieving the UN's Sustainable Development Goals (SDGs). AI makes new services possible in many domains important for the SDGs – for example:

In healthcare for SDG3, AI is being used to help offer remote health checks and follow-up tools. AI can analyse

large amounts of data to bring together insights from across large populations of patients, improving diagnosis and predictive analysis. AI has been applied with some success to models for diagnosing COVID from lung scans and imagery, or to diagnosing the 'COVID' cough from other types of coughs. AI and big data have the potential to improve healthcare systems by optimizing workflows in hospitals, providing more accurate diagnoses, optimizing clinical decision-making and bringing better treatments and higher-quality care at a lower cost.

AI BCKGROUNDER

In education for SDG4, AI is being used to monitor pupils' attention or to carry out emotional surveillance to determine how comfortable children are learning certain subjects, identifying students who are struggling before their test results become available. In many countries, AI is being used to develop personalized testing tools, to identify areas of weakness and help students improve.

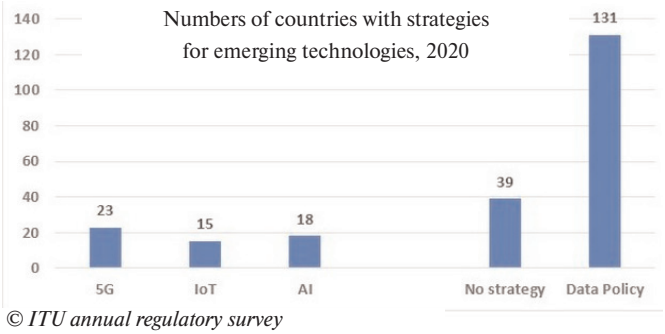
In finance, AI commonly provides insights and assistance with accounting and investment work, including automating routine tasks and uncovering new data patterns that could help with micro-investments to combat poverty (SDG1) or introduce new financial services and infrastructure (SDG9).

In manufacturing, industry and sustainable economic growth (SDG8), the use of automation, fifth generation (5G) mobile telephony, the Internet of Things (IoT) and more extensive robotics has transformed factories, supply depots and warehouses throughout Asia and Europe and the Americas, enabling more efficient and effective manufacturing, production and distribution.

Online translation and publishing software has transformed online publishing, media, and the distribution of text and materials, including books and websites. Many industries now employ chatbots and intelligent assistants to cope with routine customer queries and concerns.

In transport, AI is helping facilitate fully autonomous vehicles and autonomous driving systems (ADS), which steadily improve their driving and navigation skills through self-learning programs, as well as for real-time traffic management through urban spaces.

In agriculture, AI can be used for farm management and predictive analytics based on data from crop, soil, and weather monitoring to support decision-making and to optimize the use of resources (water, fertilizers, etc.). It can help detect pests and diseases by analysing images of plants and data on the behaviour of livestock. Agricultural robots and automation are saving labour in many resource-consuming tasks.



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ITU'S WORK ON AI

ITU is engaged in a wide range of work relating to new and emerging trends in AI, as well as helping ITU Members, Member States and stakeholders prepare for its wide-ranging policy and regulatory consequences.

The AI for Good platform [https://aiforgood.itu.int/programme/] focuses on uses of AI to help fulfil the essential needs of humanity, including achieving the 17 SDGs set out by the UN to be achieved by 2030, as an all-year, always online programme. The goal of the Summit is to identify practical applications of AI to advance the sustainable development goals and scale solutions for global impact. The Summit is organized by ITU in partnership with 38 UN sister agencies and co-convened with Switzerland.

The AI for Good YouTube channel hosts hundreds of videos highlighting interviews with AI leaders and innovators, innovations and demos showcasing AI solutions to accelerate the SDGs as a one-stop shop to catch up on emerging trends in AI for Good. Subscribe to the channel and join online for new updates and exclusive content as they go live on to explore ideas, insights and active discussions around AI to achieve the SDGs. The channel features keynotes, webinars, perspectives, an Innovation Factory and social media.

POLICY AND REGULATION

Through annual regulatory surveys and monitoring (https://www.itu.int/itu-d/sites/regulatory-market/), ITU tracks the growth of national AI strategies and policies. Machine Learning models are trained and fed by vast quantities of data, so it is vital to consider national policies in data privacy, regulation and data protection as well as approaches to the Internet of Things (IoT), sensor networks and the 5G networks making data transmission possible, when considering national approaches to AI.

According to ITU's latest Telecommunication/ICT Regulatory survey, some 18 countries had prepared specific strategies on AI by 2019, although more countries have AI sector-specific strategies, which has risen to 49 countries in 2021. However, AI encompasses diverse set of technologies, and few national strategies consider the field in total. Countries also have to consider the treatment of data flows now generated by IoT and sensor networks which feed ML models and AI technologies. Several countries, including the United States and Saudi Arabia, have prepared strategies on all three topics (5G, IoT and AI). According to the United Nations Conference on Trade and Development (UNCTAD; 2020), some two-thirds of all countries have developed policies for data protection, including AI for development.

AI IN RADIOCOMMUNICATION STANDARDS

ITU Radiocommunication (ITU-R) study groups and forthcoming reports examine the use of AI in radiocommunications:

• ITU-R Study Group 1 covers all aspects of spectrum management, including spectrum monitoring. Question 241/1 looks at "Methodologies for assessing or predicting spectrum availability".

• ITU-R Study Group 6, dedicated to broadcasting services, is studying AI and ML applications:

• Question ITU-R 144/6, “Use of AI for broadcasting", considers the impact of AI technologies and how can they be deployed to increase efficiency in programme production, quality evaluation, programme assembly and broadcast emission.

• Recommendation ITU-R BS.1387: “Method for objective measurements of perceived audio quality" about AI in the field of broadcasting.

• Report ITU-R BT.2447, “AI systems for programme production and exchange", discusses current applications and near-term initiatives, revised regularly to reflect the latest progress on AI for the applications in broadcasting.

ITU-T STANDARDS ADDRESSING AI AND MACHINE LEARNING

ICT companies in the networking business are introducing AI and ML to optimize network operations and increase energy and cost efficiency. New ITU standards provide: an architectural framework to integrate ML into 5G and future networks (ITU-T Y.3172); an evaluation framework for intelligence levels across different parts of the network (ITU-T Y.3173); and a framework for data handling in support of ML (ITU-T Y.3174. These standards originated in discussions by the ITU-T Focus Group on 'Machine Learning for Future Networks including 5G'.

The ITU-T AI/ML in 5G Challenge, introduced in 2020, rallied like-minded students and professionals from around the globe to study the practical application of AI and ML in emerging and future digital communication networks. The first edition attracted over 1,300 students and professionals from 62 countries, competing for global recognition and a prize fund of USD 36,000. By mapping emerging AI and ML solutions, the Challenge fosters a community to support the evolution of ITU standards. See the Challenge GitHub.

The ITU-T Focus Group on 'Environmental Efficiency for AI and other Emerging Technologies' aims to benchmark best practices and describe pathways towards a standardized environmental framework.

The ITU-T Focus Group on 'AI for Health', convened jointly with the World Health Organization (WHO), is working towards a framework and processes for performance benchmarking of AI for health solutions, including in response to COVID-19. It represents an open platform open to all stakeholders from different fields. The Focus Group works at the interface of multiple fields (e.g., ML/AI, medicine, regulation, public health, statistics) and includes decision-makers who value a standardized benchmarking framework. The ITU-T Focus Group on 'AI for Autonomous and Assisted Driving' is working to establish international standards to monitor and assess the behaviour of the AI 'drivers' in control of automated vehicles. The Global Initiative on 'AI and Data Commons', established in January 2020, assembles key resources for AI projects aligned with SDGs, supports rapid implementation and aims to help bring AI for Good projects to global scale.

AI and ML are widely used to construct models for the qualities of speech and other audio-visual (AV) data. An ITU-T working group on 'AI-enabled multimedia applications' (ITU-T Q5/16) is discussing standard requires for the quality assessments in AV streaming, in progressive-download and adaptive-bitrate AV (ITU-T P.1203) and video streaming (ITU-T P.1204).

New ITU-T standards address intelligent network analytics and diagnostics (ITU-T E.475) and the creation and performance testing for ML models to assess the impact of the transmission network on speech quality for 4G voice services (ITU-T P.565). Others address environmental sustainability, cable networks, and operational aspects of service provision and telecom management.

Other new ITU standards describe a datacentre infrastructure management (DCIM) system based on Big Data and AI technology (ITU-T L.1305), aiming to reduce the energy needs of datacentres, and provide the framework for a premium cable network platform to support industry in offering advanced multimedia services (ITU-T J.1600) for AI-assisted cable networks.

UN SYSTEM ACTIVITIES

In 2019 the UN Chief Executive Board endorsed the ITU-coordinated UN system-wide strategic approach and road map for supporting capacity development on AI, under the aegis of the High-Level Committee on Programmes (HLCP). HLCP has also worked on the ethics of AI, and taking into consideration the Secretary-General's Roadmap for Digital Cooperation, the 40th HLCP session decided in October 2020 to establish an HLCP interagency working group on AI (IAWG-AI), co-led by UNESCO and ITU to focus on policy and programmatic coherence of AI activities within the UN. The group leverages the stocktaking and gap analysis exercise by ITU regarding internal capacities within the UN and other stakeholders in relation to the UN system-wide strategy.

ITU has also issued the “Compendium of UN Activities on AI" as an overview of activities being carried out by the UN system. A joint effort between ITU and 37 UN agencies and bodies, all partners of the 2020 AI for Good Global Summit, resulted in an updated version of the compendium at the sixth AI for Good UN Partners Meeting, held virtually on 21 September. The 2020 Compendium covers around 260 cases and projects run by 36 UN agencies and bodies, in areas ranging from smart agriculture and food systems to transportation, financial services, healthcare and AI solutions to combat COVID-19.

CLIMATE CHANGE

OVERVIEW

Climate change has been recognized by the United Nations as “one of the greatest challenges of our time".

Given the growing proliferation of devices in our increasingly connected lives, information and communica-

tion technologies (ICTs) are part of the problem, and responsible for a growing amount of carbon emissions and e-waste.

ICTs can also contribute to reducing carbon emissions as part of the solution – for example, through 'dematerialization' (e.g. replacing books with digital books) or through substitution (e.g. replacing travel for meetings with participation in teleconferences).

The 'value' of an ICT service should not necessarily be measured in terms of its popularity, consumer convenience or carbon footprint. Many ICT services have vital benefits. For example, various ICT services are used for monitoring storms and measuring climate change.

ITU works on addressing climate change due to ICTs and through ICTs. Work includes a broad portfolio of activities in e-waste; identifying the standardization needs to develop a sustainable approach to artificial intelligence and other emerging technologies; and supporting the growth of satellite surveillance and monitoring services from space for, for example, more accurate weather forecasting and prediction of extreme weather events linked to climate change, and particularly for predicting the strength, path and location of landfall of tropical storms.

ITU's work on addressing climate change contributes towards SDG 13: climate action, as well as the goals for life below water (SDG 14) and life on land (SDG 15).

CHALLENGES

The United Nations Framework Convention on Climate Change (UNFCCC) defines climate change as "a change of climate that is attributed directly or indirectly to human activity that alters the composition of the global atmosphere and that is in addition to natural climate variability observed over comparable time periods". The Intergovernmental Panel on Climate Change (IPCC) defines climate change as a "change in the state of the climate that can be identified (e.g. using statistical tests) by changes in the mean and/or the variability of its properties, and that persists for an extended period, typically decades or longer. It refers to any change in climate over time, whether due to natural variability or human activity". The 2030 Agenda acknowledges climate change as "one of the greatest challenges of our time" [8]. It elaborates that climate change and "its adverse impacts undermine the ability of all countries to achieve sustainable development. The survival of many societies, and of the biological support systems of the planet, is at risk" [9].

According to NASA, the immediate signs of climate change include: global temperature rise; warming oceans; ice sheet and glacial retreat; decreasing snow cover; sea level rise; declining Arctic sea ice; extreme weather events; and ocean acidification [10]. Many of these consequences of climate change are monitored using satellite imagery from outer space.

No matter where you live, everyone stands to be affected by the consequences of climate change. Some 2.4 million (40%) of the total world population live within 100km of the coast today, with at least 11-15% of the population of small island developing states (SIDS) living on land with an elevation of 5 meters or lower [11]. The World Bank identifies that cities are also increasingly at risk from the impacts of climate change, with more than 80% of the global costs of adaptation to climate change expected to be incurred by and within cities.

OPPORTUNITIES

ICT products and services consume energy, that generates carbon emissions over their life cycle in:

a) Manufacturing and production: It has been estimated that a tonne of laptops could be responsible for emissions of up to 10 tonnes of carbon dioxide [12].

b) Usage:

Growth in number of consumer devices: Cisco estimates that nearly 650 million mobile devices and connections were added in 2017 [13]. The Organisation for Economic Co-operation and Development (OECD) estimates that a typical OECD household with two children may now have up to ten connected devices on average per household [14].

Data flows: Cisco, for example, estimates that global mobile data traffic grew by 71% in 2017. Global mobile data traffic reached 11.5 Exabytes per month at the end of 2017, up from 6.7 Exabytes per month at the end of 2016 [15].

Energy use & efficiency across networks: Standards can help address these concerns by providing common measurement methodologies. ITU has developed KPIs for measuring carbon footprint, energy performance and efficiency across telecom/ICT networks – see below.

Data centres: The number of data centres is increasing rapidly worldwide, with a large number of data centres being installed in Scandinavia (e.g. Iceland), where average temperatures are lower. Data centres vary in their energy efficiency and energy sources, with some powered by renewable energy [16].

c) Disposal: In early 2019, the United Nations found that US$62.5 billion dollars in materials are lost in approximately 50 million tonnes of annual e-waste, which could be tripled by 2050[17].

The installation of 'smart infrastructure' allows to improve monitoring and evaluation of energy consumption across networks in real-time. For example, smart electricity meters can help building-owners and occupiers understand their energy consumption better. Advanced computer modelling can help telecom operators plan for and handle data traffic more efficiently. Smart traffic lights can help reduce traffic jams and greenhouse gas emissions and pollution from cars.

In fact, the carbon footprint of ICT goods and services depends in large part on how/where energy is generated and whether power is generated from fossil fuels or renewable energy sources. Renewable energy sources are not de facto clean energy sources in terms of carbon footprint – although they are cleaner. Carbon-fueled power stations emit 820g equivalent of CO2 equivalent per kWh of energy, gas-fired power stations 490g equivalent of CO2 equivalent per kWh of energy, photovoltaic sources 41, hydraulic energy 24, nuclear power stations 12 and wind-powered stations 11 gCO2eq per kWh [18].

ITU'S CONTRIBUTION

Various ICT services are useful for monitoring climate change and storms (e.g. better modelling and prediction of weather and of climate, space-based observation of greenhouse gas emissions or GHGs). ITU supports the growth of

satellite surveillance and monitoring services from space for:

Monitoring GHG emissions and pollution;

Improving climate modelling and prediction of trends;

Forecasting weather more accurately and predicting extreme weather events linked to climate change.

ITU-R Working Party 7B (WP 7B) studies space radiocommunication applications relevant to climate change. ITU-R Working Party 7C (WP 7C) studies the remote sensing systems that are important for monitoring and tracking the extent, pace and acceleration of climate change.

ITU-T Study Group 5 studies 'Environment, climate change and circular economy'. The group has been working on developing international standards (i.e. ITU-T Recommendations) that support the sustainable use of ICTs (including products, services, installation, infrastructure, etc.). Recently, Study Group 5 is working to align the development of ICTs with the UN 2030 Agenda for Sustainable Development and the UNFCCC Paris Agreement.

Recognizing the growing footprint of digital technologies, ITU has also created the new Focus Group on "Environmental Efficiency for AI and other Emerging Technologies". This focus group will study the environmental performance of AI, Big Data application, blockchain and other digital technologies. The group will identify the standardization needs to develop a sustainable approach to AI and other emerging technologies. ITU published a report, entitled "Turning digital technology innovation into climate action", to highlight the emerging role of digital technologies in accelerating climate actions and tackling the e-waste challenge. With other UN partners, ITU also recently published the report, "Frontier Technologies to Protect the Environment and Combat Climate Change" (2020).

The United for Smart Sustainable Cities (U4SSC) initiative is a UN initiative coordinated by ITU and UNECE with the support of 14 other UN agencies and programmes. The initiative is dedicated to support the transition to smart sustainable cities and is developing technical reports and deliverables that encourage circularity actions in cities and examine the impacts of frontier technologies in cities.

In addition, ITU organizes multi-stakeholder events to highlight the role of ICTs in climate change. With eight other UN agencies and programmes, ITU hosts a Symposium on ICT, Environment & Climate Change [19] regularly, which brings together leading telecom executives, policy-makers, service providers, civil society, the academia and UN representatives to discuss how frontier technologies can help combat climate change. ITU also organizes the Green Standards Week every year to debate key issues relating to ICT standards and the environment. This event brings together the ICT sector, policy-makers, city planners, representatives from civil society, the academia and technical experts to share experiences in building smart sustainable cities and how standards can improve the sustainability of different sectors.

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