AN EXPERIMENTAL VERIFICATION OF NEW NON-QUASI-STATIC SMALL-SIGNAL MOSFET MODEL

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ABSTRACT

This article presents the results of an experimental verification of the New Non-Quasi-Static (NQS) Small-Signal MOSFET Model proposed in [1,2]. This model is valid in all operating modes, from weak to strong inversion and from nonsaturation to saturation. For the purpose of verification test transistors with de-embedding, dummy structures in 0.35 m technology were designed. The procedure of de-embedding was based on the open-short [3] method, optimised for RF measurement up to 30 GHz. The results obtained have confirmed aplicability of the model for the small-signal MOSFET simulation.

KEYWORDS: _Semiconductor device modeling, RF IC Design, CMOS and BiCMOS circuit simulations, circuits for communications._

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I. INTRODUCTION

Small-signal MOSFET model and clear procedure of parameters extraction are needed to successfully design analog radio frequency integrated circuits (RFIC). When the device operates near or above the cut-off frequency, the NQS effects are strongly important. However, most models available in SPICE use the quasi-static (QS) formulation [4] which can result in unpredictable behavior of high-frequency circuits. QS approximation assumes the movable carriers in the channel of the transistor respond instantaneously to perturbations induced by a time-varying external signal, thus the channel charge achieve equilibrium once bias is applied.

As a result, serious inconsistencies arise when the QS approach is used to RF MOSFET modeling. For instance, according to the models presented in [5] magnitudes of transadmittances of voltage-controlled current sources tend to infinity as frequency increases. It is worth mentioning that any charge–based model, such as BSIM3v3, MOS Model 9 or EKV is inherently composed of such current sources as those in [5].

Also, for frequencies much smaller than the transistor cut-off frequency, NQS effects can occur. When an inductive load tunes out capacitance at some node, transistor behavior QS prediction can fail. Especially, PMOS devices can suffer from NQS effect because of lower holes mobility. Sometimes, it is possible to find an extremely long channel device, like 100μm with cut-off frequency below 1MHz where NQS effects can occur for low-frequencies [6].

The purpose of this work is to briefly present the results of an experimental verification in 0.35μm technology of the new NQS model, which was presented during 1st IEEE International Conference on Circuits and Systems for Communications in St. Petersburg, Russia [2]. We investigated admittance parameters of the measured test transistors and compared them to model simulation results. The experiment design and procedure of model parameters extraction are presented here.

II. NQS MODEL OF THE MOS TRANSISTOR [1-2]

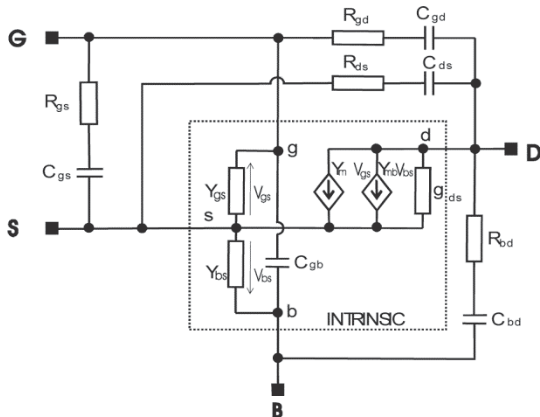

Fig. 1. Small-signal equivalent circuit of the MOSFET, with subcircuit enveloped in dotted line being the intrinsic part of the transistor

The equivalent circuit presented in the picture is simplified as compared to the one showed in [2] due to application of de-embedding strategy that allow us to reject the impact of pad parasitics. The set of equations establishing the model is as follows:

$$\mu(E_0) = \frac{\mu_0}{[1+(E_0/E_C)^{\beta}]^{1/\beta}}, \left(E_0 = \frac{|V_{DS}|}{L}\right), \quad (1)$$

$$C_{gb} = \frac{g_m \eta L}{(1+\eta)\mu(E_0)E_0}, \left(\eta = \frac{g_{mb}}{g_m}\right), \quad (2)$$

$$Y_{mg} = g_m \exp(\gamma L), \; Y_{mb} = g_{mb}\exp(\gamma L), \quad (3)$$

$$Y_{gs} = j\omega \frac{C_{gb} D_C [\exp(\gamma L) - 1]}{\eta \gamma L (1 - \gamma V_T / E_0)}, \quad (4)$$

$$Y_{bs} = \eta^2 Y_{gs}, \quad (5)$$

$$\gamma = \frac{1}{2}\left(\frac{E_0}{V_T} - \sqrt{\frac{\sqrt{a^2+b^2}+a}{2}} - j\sqrt{\frac{\sqrt{a^2+b^2}-a}{2}}\right), \quad (6)$$

$$a = \left(\frac{E_0}{V_T}\right)^2, b = \frac{4\omega(1+D_C)}{V_T \mu(E_0)}, V_T = \frac{kT}{q}. \quad (7)$$

where μ_0, EC and E0 are, respectively, the low-field mobility, the characteristic field, and the static longitudinal electric field at the Q-point. gds, gm and gmb are the QS drain-source conductance, gate transconductance and bulk transconductance.

For intrinsic part of the transistor we have $y_{12} = 0$. The intrinsic MOSFET without parasitics has to be unilateral ($y_{12} = 0$) for the reason that charge carriers (electrons or holes) are only injected through the source-channel barrier potential. When frequency goes to infinity, magnitude of transadmittance y_{21} goes to zero, and phase is linearly delayed. Transadmittance y_{21} predicted by the model behaves similarly to complex attenuated sinusoid, which was verified by experiment.

III. EXPERIMENT

To verify the model designed were eight test transistors in 0.35μm technology with geometries as follows (L denotes the channel length in μm, W – the channel width in μm, F – the number of fingers): (1) L=0.35 W=50 F=5, (2) L=0.5 W=50 F=5, (3) L=0.7

W=50 F=5, (4) L=1.4 W=50 F=5, (5) L=0.35 W=100 F=10, (6) L=0.5 W=100 F=10, (7) L=0.7 W=100 F=10, (8) L=0.35 W=200 F=20. The transistor geometries were optimized for DC measurement of the drain current with swept gate-source VGS, drain-source VDS and bulk-source VBS voltages and RF scattering parameters measurement of the transistor in common source configuration through Air Coplanar Probes. The strategy of de-embedding was based on the widely used open-short method [3].

Although transistor layouts provided possibility of drain current measurement with swept bulk-source voltage, short between bulk and source for RF measurement was obtained using ground of probes. Based on RF measurement of the short dummy structure, there were extrapolated values of the bulk and source inductance Lpar and resistance Rpar to ground in common source configuration. These elements cannot be removed from the device under test through de-embedding and had to be included in simulations of the model.

To obtain reliable and repeatable measurements four samples with described above eight transistors were measured. RF measurements were performed based on two different calibration techniques of the network vector analyzer (NWA). Two samples were measured making use of SOLT calibration method [3] in the 65MHz – 25GHz frequency range and other samples were measured making use of LRM method [3] in the 65MHz – 30GHz frequency range. The impedance substrate standard (ISS) was used to calibrate the NWA. Transmission lines on ISS were used to verify the quality of calibration. For all samples, it was obtained almost the same results, which eliminates risk of one-time wrong measurement. The procedure of transistor de-embedding was verified positively for all samples by measurement and de-embedding of known thru lines. Also, the characteristics obtained from the magnitude of hybrid h21-parameter let us treat measurements as reliable in the investigated frequency range. Transistors were measured at twenty four Q-points, V_{DS}[V]=0, 0.3, 0.6, 0.9, 2.1, 3,3 and V_{GS}[V]=0.9, 1.0, 1.1, 1.2.

In Fig. 2 and 3 shown are representative results, respectivelly, y12 and y21 transadmittances for 50μm-channel width transistors at Q-point VDS=3.3V and VGS=1.2V. gds, gm and gmb parameters were extracted through DC measurement and EC and μ values were taken from IC manufacturer data. Other values of the model parameters were obtained by manual curve-fitting of admittance experimental and simulated frequency characteristics. At first, real(y21) was fitted, which was aimed to obtain similar characteristic slope (L[μm]=0.35, 0.5, 0.7) or period for long channel transitor (L[μm]=1.4). Value of coupling parameter DC was extracted in this step. Afterwards, imag(y21) and imag(y12) were fitted by Cgd capacitance tuning. At VDS[V]=0.6, 0.9, 2.1, 3,3 Q-points, real(y12) was near to zero which agree with y12=0 thesis for intrinsic transistor. At these Q-points, extracted Rgd-resistance value was equal to zero. An increase in real(y12) for higher frequencies is a result of described above bulk-source short through ground of the measurement system. At VDS[V]=0, 0.3 Q-points it was necessary to tune Rgd to value different than zero, because of large decreasing tendency of real(y12) with frequency. In the next step, y11 characteristics were fitted, accurate fitting was obtained by Cgs and Rgs parameters tuning. Afterwards, it was possible to perfectly fit y22 characteristics through Cds, Rds and Cbd, Rbd tuning. In Fig 4 shown are representative results, respectivelly, y11 and y22 admittance parameters for transistor with L=0.35μm, W=50μm at Q-point VDS=3.3V, VGS=1.2V. Extracted parameter values for described transistors at Q-point VDS=3.3V and VGS=1.2V summarized are in Table.1.

IV. CONCLUSIONS

We presented the results of an experimental verification of the MOSFET model , we had proposed previously. The experimental results show that y21 MOSFET transadmittance vs. frequency behaves in fact like an attenuated complex sinusoid for long channel device (L=1.4μm), see Fig.3, which was theoretically predicted by the model. Of course, investigated frequency range is much wider than presented transistor cut-off frequency (fT=2.2GHz). The experiments also confirm real(y12)=0 at Q-points VDS[V]=0.6, 0.9, 2.1, 3,3 which agrees with thesis on y12=0 for intrinsic transistor. A simple parasitics circuit proposed in Fig.1 provides close fitting between measured and simulated y11 and y22 admittance characteristics. The model is in good agreement with the experimental results and does not have physical inconsistencies unlike other models.

Table 1

Extracted small-signal model parameters of 50μm-width transistors at Q-point V_{DS}=3.3V and V_{GS}=1.2V, other parameters: W=50um, F=5, β=2, E_C=2.812·106V/m, μ_0=475.8cm2/V/s, T=27°C, R_{gd}=0Ω, R_{par}=411mΩ, L_{par}=29.18pH; the cut-off frequencies are shown in the last row

	L=0.35um	*L=0.5um*	*L=0.7um*	*L=1.4um*
g_m[mS]	9.99	7.684	5.822	3.236
g_{mb}[mS]	2.206	2.085	1.644	0.9488
g_{ds}[uS]	532	250	152	48
D_C[10^{-3}]	886.6	477.5	322.6	468.1
C_{gd}[fF]	8.433	9.57	9.863	14.16
C_{gs}[fF]	33.72	62.63	96.65	148.6
C_{ds}[fF]	22.18	20.8	20.8	20.8
C_{bd}[fF]	20.75	18.58	18.58	23.17
R_{gs}[Ω]	111.5	54.24	43.85	49.09
R_{ds}[Ω]	17.54	23.17	6.531	38.31
R_{bd}[Ω]	580.8	724.4	981.7	3020
f_T[GHz]	25.8	14.3	8	2.2

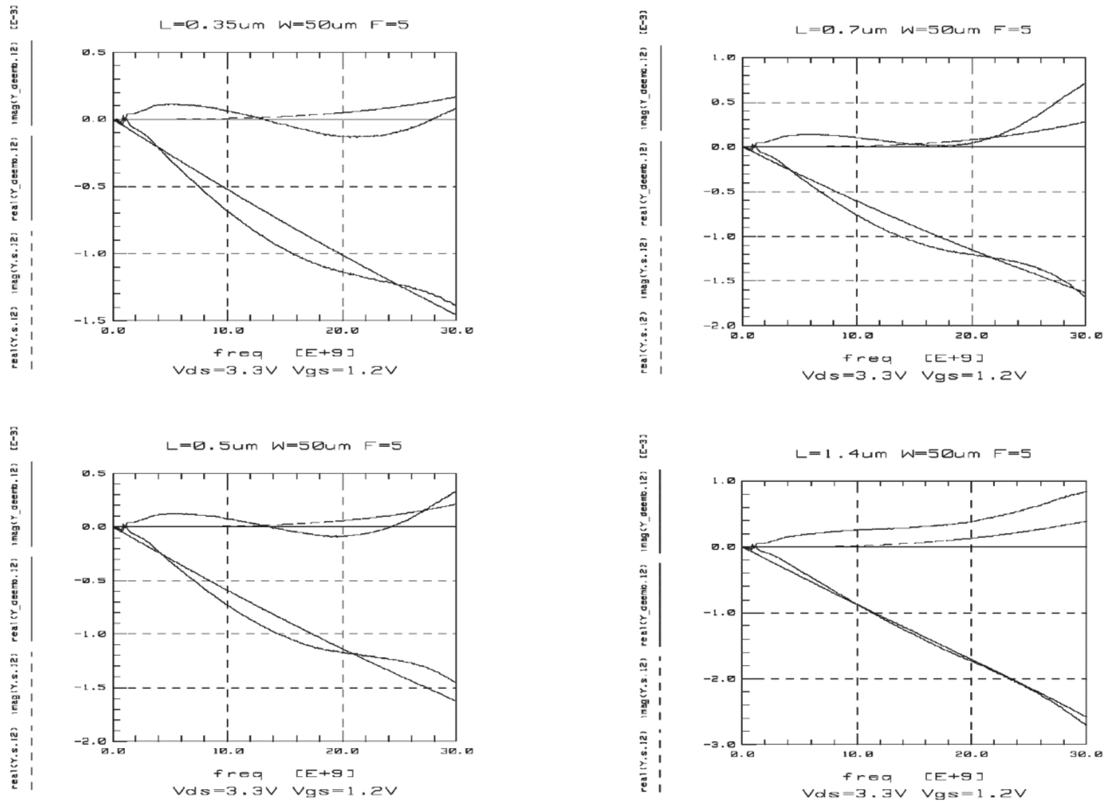

Fig. 2. Comparison between measured and simulated y12 parameters for transistors with L[μm]=0.35, 0.5, 0.7, 1.4, W=50μm (V_{DS}=3.3V , V_{GS}=1.2V)

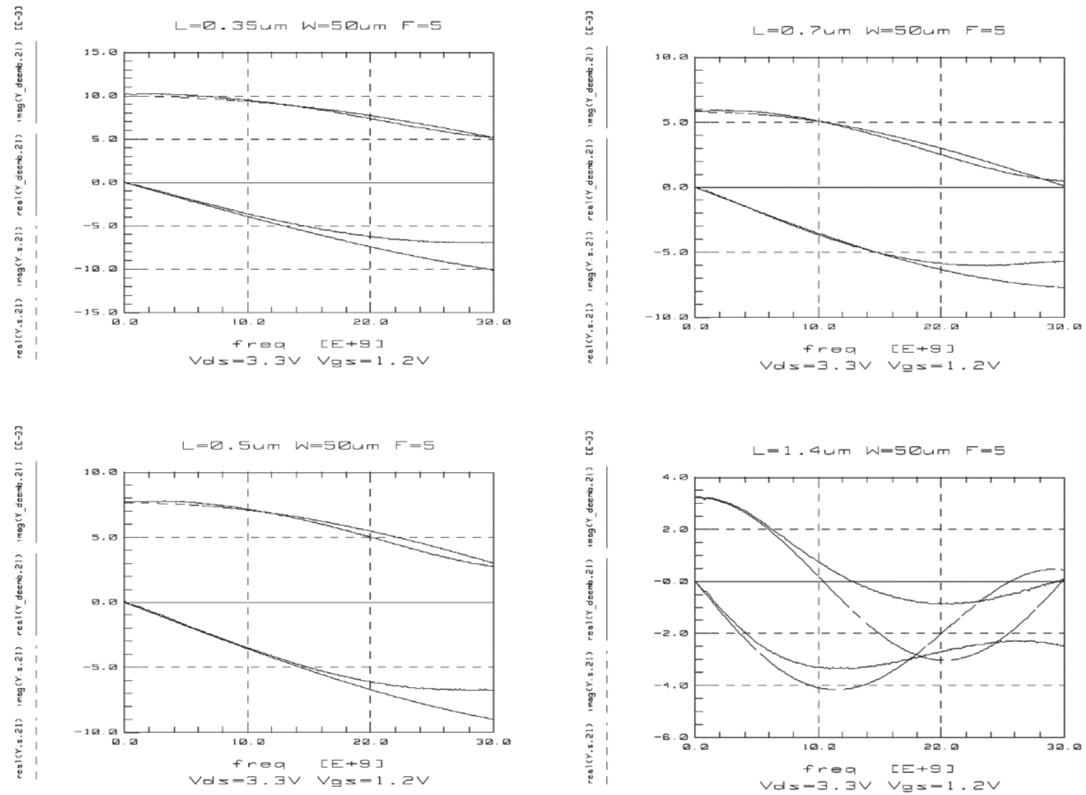

Fig. 3. Comparison between measured and simulated y21 parameters for transistors with L[μm]=0.35, 0.5, 0.7, 1.4, W=50μm (V_{DS}=3.3V , V_{GS}=1.2V)

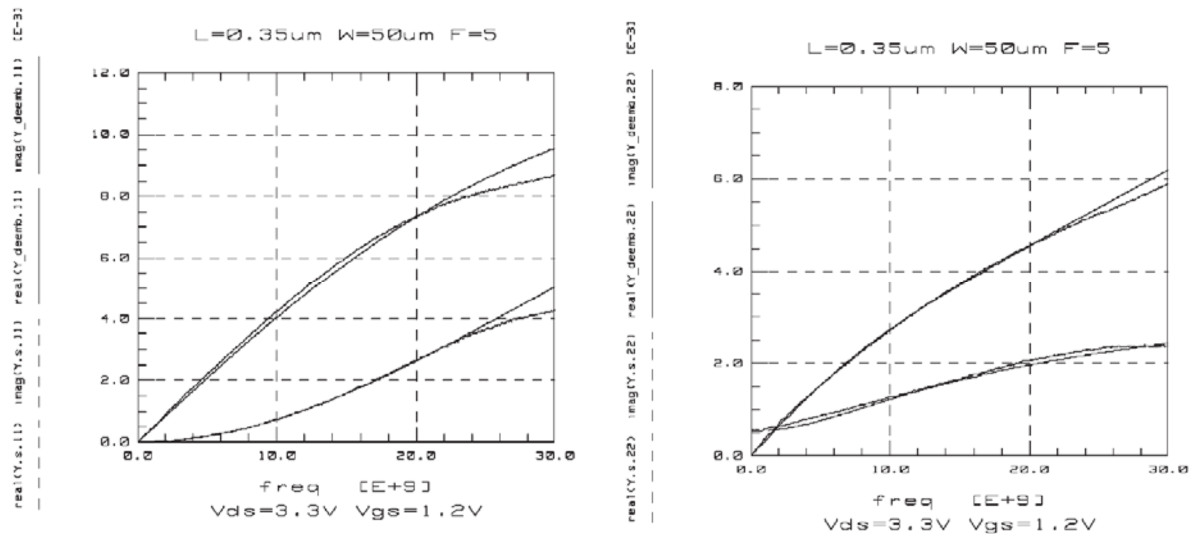

Fig.4. Comparison between measured and simulated y11 and y22 parameters for transistor with L=0.35μm, W=50μm (V_{DS}=3.3V , V_{GS}=1.2V)

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