A 36 MW, 13 B, 2.1 MS/S MULTI-BIT ΔΣ ADC IN 0.18 M DIGITAL CMOS PROCESS USING AN EFFICIENT TOP-DOWN DESIGN METHODOLOGY

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DOI: 10.36724/2664-066X-2021-7-4-7-11

ABSTRACT

A systematic method to design a switched-capacitor (SC) multi-bit ΔΣ ADC integrated circuit is presented. The modulator consists of a fourth-order, multi-stage (2-1-1) architecture, with a 3-bit fash ADC in the last stage only. The modulator building blocks specifcations were designed using a systematic top-down methodology. Trade-offs between circuit building block specifcations, optimization time and computing resources are derived. When sampled at 50 MHz, measured performance reveals an 81.3 dB dynamic range for an output Nyquist rate of 2.1 MS/s while using a single 1.8 V supply and dissipating 36 mW of power.

KEYWORDS: *switched-capacitor, multi-bit fash ADC, optimization time, computing resources, digital CMOS technology.*

The article is reworked from unpublished 2nd IEEE International Conference on Circuits and Systems for Communications (ICCSC) materials.

I. INTRODUCTION

Delta-sigma modulators (ΔΣMs) constitute an essential block in mixed-signal designs. The increasingly stringent requirements of today's communication systems and portable devices are however rendering the design of those ΔΣMs more challenging. Extending the input frequency range to exceed the 1 MHz range, while maintaining a feasible sampling frequency is further rendered more complicated by the ever shrinking transistor dimension, and in turn, the supply voltage. The above two challenges are causing ΔΣMs to suffer from a long design cycle increasing therefore its time-to-market.

Synthesizing the modulator's main building block specifications on the system level is an efficient design method that has been suggested in the literature [1]-[3]. In this paper, an observation of the weak correlation among the parameters to be synthesized allows for the deduction of a fast synthesis method using Matlab/Simulink [4]. Parameters dictating the final performance of the modulator were separated reducing the complexity of the algorithm from exponential to linear dependency on the variables. In other words, the complexity of the algorithm used to deduce the optimum parameters, assuming n parameters exist, is reduced from On() to ·nO1(). Long optimization time could therefore be avoided and simple sweeps on the key parameters were enough to determine blocks' specifications on the system level.

This method will be demonstrated efficient in the implementation of a well-performing modulator. This paper is organized as follows: A detailed description of the system-level design of the modulator follows in section 2. The circuit implementation and experimental results from the fabricated IC are presented in sections 3 and 4 respectively. Concluding remarks are given in the last section of this paper.

II. SYSTEM-LEVEL DESIGN

2.1. Architecture

The selection of the architecture is the first step in the system-level design. In order to achieve a large dynamic range, a detailed study for the choice of the appropriate topology and proper topology parameters was outlined in [5][6]. Therefore, the assumption for the remainder of this paper is that the architecture is already selected. The focus will be on the impact of the circuit non-idealities on the system performance.

In order to meet the goal specifications: minimum of 14 bits of resolution for ~ 1 MHz input bandwidth, a 4th order, single-bit, cascade 2-1-1 architecture with a 3-bit quantizer in the last stage and 50 MHz sampling frequency, fs were chosen.

2.2. Non-Idealities Considered

The complete system-level representation of the non-ideal model of the integrator was achieved in Matlab/Simulink. The inputs to this block include but are not limited to the following non-idealities: operational transconductance amplifier (OTA) DC gain, unity-gain bandwidth (BW), slew rate (SR), input thermal noise density (S_n), switch on-resistance (R), and sampling capacitor (Cs). Other constants include the system oversampling ratio, OSR, Boltzman's constant (K) and the temperature (T). The comparator offset is another parameter that was included in the non-ideal characterisation of the modulator, even though noise-shaping alleviates its degradative effect on the overall system performance.

A description of the effect of each one of those non-idealities on the overall system performance is presented next. In this paper, the choice was made to carry out the optimization for parameters such as OTA DC gain, BW, SR, etc., rather than parameters such as OTA differential pair transconductance, output impedance, and biasing current, as was done in [2]. The latter method assumes an op amp topology constraining therefore the mapping of the obtained results to any other topology. The effect of each circuit non-ideality is explained next.

The OTA thermal noise is computed using a 2-pole system approximation. The root-mean-squared, RMS input-referred thermal noise is then given by

$$\sqrt{(S_n \cdot BW)/(2A)},$$

where A represents the finite DC gain of the OTA.

The switched- capacitor (also knows as KT/C) noise is computed according to

$$\sqrt{(K \cdot T)/(C_s \cdot OSR)}.$$

The distortion due to the front-end switches were deduced separately. The switches of the front-end sampling network introduce distortion due to the dependency of their on-resistance on the input voltage. The worst-case distortion due to the variation in the resistance of the input switches was quantified in [2] and is given by:

$$THD = e^{[-4R \cdot C_s \cdot f_s]^{-1}} / \left(1 - e^{[-4R \cdot C_s \cdot f_s]^{-1}}\right), \qquad (1)$$

where THD stands for the total harmonic distortion.

A plot of the magnitude of the THD,|THD|, as a function of the witch on-resistance reveals that in the case where C_s = 1 pF, f_s = 50 MHz and a maximum allowable distortion of 80 dB, a maximum switch on-resistance, R_{max} of 540 Ω is allowed.

All the previously mentioned inputs were then added together, with an input saturation block to represent the limited input swing of the OTA, to constitute the input to a modified delayed-integrator transfer function. The finite DC gain of the OTA, A, as well as capacitor ratio mismatch denoted by *a*, will transform the transfer function from the ideal $1/(z-1)$ transfer function for a delayed integrator to:

$$1LSB = (V_{FS+} - V_{FS-})/(2^N - 1). \quad (3)$$

The limited OTA SR and BW were also modeled using a Matlab function that computes the current output given a current input, previous output and three cases which are determined by a purely slewing behavior, purely exponential behavior or a combination of both. A Matlab function is dedicated to compute the output value after checking for each one of the three cases.

Finally the OTA output limited swing is modeled by a saturation block at the output of the modulator.

Accounting for all the non-idealities discussed above will transform the transfer function of the integrator from a single-input, single-output transfer function given by $1/(z-1)$ to a more complex model which was generated in Simulink and Matlab as mentioned earlier.

In order to study the simultaneous effects of some of the circuit non-idealities on the system's performance, 3-D simulation sweeps on the key non-idealities were carried out. Observations of the results shown in Figure 1 reveal that little correlation exists between the swept variables. The absence of maxima in the plots reveals that no one optimum solution exists, rather, the plots can be used to find the minimum specification needed for each one of the swept variables to meet the desired SNR. As an example, a plot of the SNR (where noise throughout includes harmonic bins) as a function of the OTA thermal noise density, S_n and BW is shown in Figure 1 (b). The monotonically increasing plots imply that these parameters could be considered uncorrelated over a practically large range of OTA BW and S_n. Similar conclusions could be drawn when observing the other plots in Figure 1, hence the validation of the separation of variable method, with the exception of BW and SR which both determine the settling behavior of the OTA and need to be swept simultaneously.

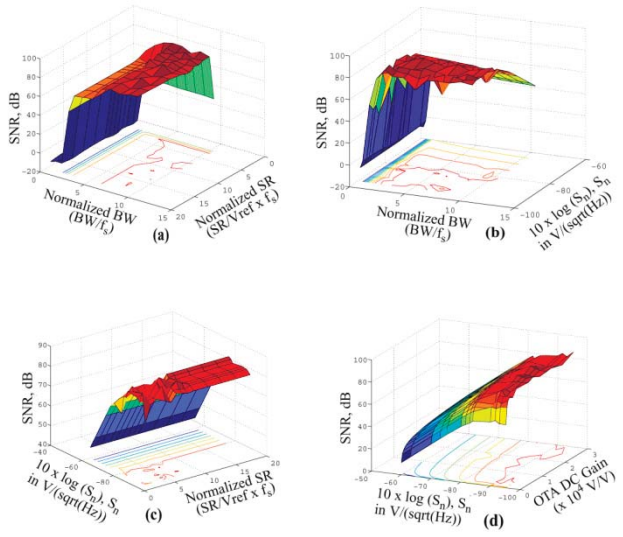

Fig. 1. Peak SNR versus: (a) BW and SR, (b) BW and S_n, (c) SR and S_n and (d) DC Gain and S_n

The above observation eliminates the need for a time-consuming, difficult-to-setup multi-dimensional optimization.

The difficulties associated with setting up multi-dimensional optimization and selecting a set of good initial conditions for convergence purposes could also be avoided. Instead, 1-D sweeps on each circuit non-ideality separately is enough for all practical purposes to deduce a set of specifications that will eventually be mapped into a transistor-level system.

In [7], the method presented above was used to design a single-bit ΔΣ ADC. The aim of the current work presented in this paper is to extend those results to include multi-bit modulators for higher achievable resolution. A complete section is therefore devoted for discussing the DAC non-linearities and their effect on the system performance, and is presented next.

2.3. DAC Non-Idealities in Multi-bit Quantization

As mentioned earlier, with multi-bit quantization, the DAC linearity becomes a concern when high resolution ΔΣ ADCs are required. If the DAC exhibits non-linearities that exceed the overall system linearity requirement, then the converter will be limited to the DAC accuracy. Different calibration techniques were proposed in the literature to improve the performance of the internal DAC through the use of individual level averaging, data weighted averaging, and other modified versions of the previous methods. Each one of those proposed methods has advantages and disadvantages which won't be discussed here.

One common feature to all these correction techniques is that they improve the DAC linearity at the expense of additional power dissipation. For the design under consideration, and in order to keep the power dissipation to a minimum, system-level simulations presented next will show that the required DAC Integral-Non-Linearity, INL is believed to be met with a simple resistor string and careful resistance choice and layout techniques. Note that multi-bit quantization in the last stage only was used as explained in great details in [6].

The effect of the DAC INL on the overall dynamic range of the modulator was simulated in Matlab/Simulink. The reference voltages in both the ADC and DAC of the last stage of the modulator were deviated from their ideal levels. To do so, an additive noise source having a Gaussian distribution, with variance (noise power) swept between 0 LSB (ideal DAC curve) and 1 LSB, where LSB = Least Significant Bit, and defined as:

$$1LSB = (V_{FS+} - V_{FS-})/(2^N - 1). \quad (3)$$

The DAC INL was then calculated using the best-fit line method. The results of the selected INL curves and the corresponding SNDR as a function of input power of the modulator are shown in Figure 2.

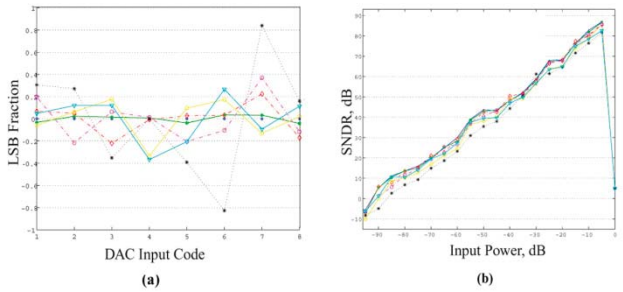

Fig. 2. (a) INL for different non-ideal DAC transfer curves and (b) corresponding SNDR

From the plots, it can be seen that provided that the maximum DAC INL is limited to 0.15 · LSB, the achievable resolution is ~ 14 bits.

2.4. Building Block Specifications Synthesis

Based on the observation of the little correlation existing between the variables, specifications on the building blocks were deduced using 1-D sweeps only. One variable representing one circuit non-ideality was swept at a time, while the other variables were made ideal.

Plots of the SNR versus different circuit non-idealities were all found to be monotonic, as expected. The minimum OTA DC gain, BW, SR, input thermal noise density, comparator offset as well as the input switching network time constant could therefore be deduced. The DAC maximum allowable non-linearity could be deduced from Figure 2.

III. SC CIRCUIT IMPLEMENTATION

3.1. Operational Transconductance Amplifier

A single-stage folded-cascode topology was used for the implementation of the OTA due to its excellent frequency characteristics. A complementary differential pair at the input was used in order to allow for a larger input swing. Gain boosting were added to the output stage in order to increase the OTA DC gain. Pole-zero modeling of the OTA was performed in order to choose the optimum biasing and transistor sizing while meeting the stringent requirements using a single 1.8 V supply and minimum power dissipation. A switched-capacitor common-mode feedback circuit was used due to its low power dissipation. The optimized OTA achieves 100 dB DC gain. When loaded with 1.5 pF capacitive load, the OTA achieves 410 MHz unity-gain bandwidth, a phase margin of 58°, and 236, 246 V/μs rising, falling slew rates respectively.

3.2. Comparator & Multi-bit Quantizer

A CMOS dynamic comparator and a clocked RS latch were used to implement the 1-bit quantizer. In the case of the multi-bit (3b) quantizer in the last stage, a flash ADC comprising of 7 dynamic CMOS comparators was used. The reference voltages were generated using a resistor string, and a switched-capacitor arrangement to carry out the subtraction between the reference levels and the integrator outputs [8]. The resistor values had to be chosen small enough to avoid long settling time, but large enough to minimize power dissipation. Values chosen for the resistors also have an impact on the matching which directly affects the resolution of the multi-bit ADC/DAC.

As explained earlier, the INL of the DAC had to be kept below 0.15 · LSB. Assuming a 3-bit DAC with full swing range of about 0.5 V, and using (3), we get that the noise on the DAC reference voltages due to mismatch in the resistor values generating those levels (as well as some other noise sources such as substrate noise) have to be kept below 10.7 mV. Since it is only matching between resistors and not absolute values that matters, with proper layout techniques, the matching between any two or more resistors could be made as small as 0.01% (1%being an achievable mismatch ratio with moderate layout techniques) [9].

Even with a moderate matching of 1% between the various resistors, the INL requirement of 10.7 mV is achievable with a simple resistor string.

It is worth mentioning that the choice of the resistor layout dimensions (width and length) also affects the matching percentage between two or more resistors due to process variations. All of the above considerations were taken into account when the resistors were laid out in order to minimize the process variation effects controllable by proper layout techniques. The final resistance choice was set to 200 Ω.

No pre-amplification stage was used for the comparator due to the its relaxed offset requirements. The implemented comparator achieves a resolution equivalent to 11 bits, capable therefore of resolving a differential signal of ~880 μV.

3.3. Switches

The switches were implemented using regular transmission gates. Despite the low voltage used to clock the gates of the switches, sizing the NMOS and PMOS according to (1) will limit the distortion of the front-end sampling network to an allowable level.

3.4. Other Blocks

The four-phase non-overlapping clocks were generated on-chip, from a single off-chip clock. Delayed versions of the clocks (together with fully differential implementation) were used to minimize charge injection. Both clocks and their complementary signals were generated for both the NMOS and PMOS transistors of the switches. Buffers appropriately sized for driving the clock line capacitive load with fast rise/fall times were inserted at the clock outputs.

The overall SC circuit is shown in Figure 3, and its mapping into a 0.18 μm, single-poly, 6-metal CMOS process IC is shown in Figure 4. Post-layout simulations were performed on the IC and it is worth mentioning that no transistor-level iterations were needed since no performance degradation in the SNR between the non-ideal system (Simulink) and transistor-level system (Cadence) were observed.

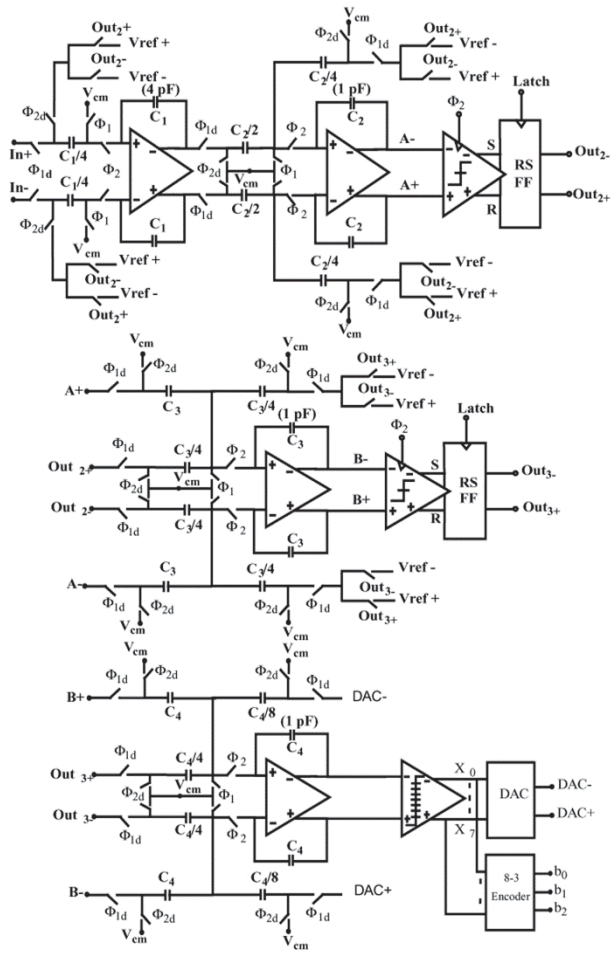

Fig. 3. SC implementation of the multi-bit modulator

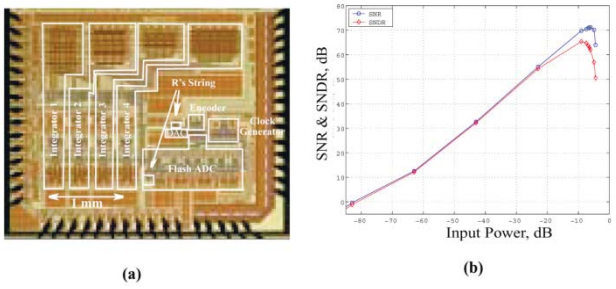

Fig. 4. IC (a) microphotograph and (b) measured DR

IV. EXPERIMENTAL RESULTS

A four-layer printed circuit board was used to test the IC. Separation of analog and digital planes, de-coupling capacitors and voltage regulation for the supply voltage lines were included. The differential input was generated using a Teradyne A567 mixed-signal tester and the clock using a Hewlett Packard high-quality pulse generator model number 81130A. The achieved dynamic range, DR shown in Figure 4 (b) is 13.2 bits of resolution. Table 1 summarizes the measured specifications of the IC.

V. CONCLUSIONS

We have presented the implementation and experimental results of a performing multi-bit ΔΣ ADC in 0.18 μm digital CMOS technology. Careful system-level modeling and synthesis of circuit specifications were used to minimize the power dissipation. It was shown that assuming independency among the circuit non-idealities and optimizing for each separately can provide a practical means for achieving a target specifications in the presence of complex and unpredictable interactions between the non-idealities. Experimental results agreed to some extent with the system-level modeling. The expected dynamic range was 14 bits while experimental results showed a resolution of 13.2 bits. Verification of the system-level modeling method was also conducted on a single-bit modulator, revealing even closer matching between expected and experimental results, justifying further the usefulness of the proposed method.

Table 1

Summary of measured specifications

Technology	0.18μm CMOS	***Output Rate***	~ 2 MS/s
Supply	1.8 V	***Ref. Volt.***	1.8 V, 0 V
Core Area	2.55x2.3 mm^2	***Input Range***	1.5 V_{p-p}
Power	36 mW	***DR***	81.3 dB
f_s	50 MHz	***Peak SNR***	72.7 dB
OSR	24	***Peak SNDR***	65.7 dB

ACKNOWLEDGMENTS

This work was supported by Micronet, a Canadian network of centres of excellence dealing with microelectronic devices, circuits and systems and the Canadian Microelectronics Corporation.

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