LOW COST IC TESTER USING PSEUDO-RANDOM APPROACH

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ABSTRACT

Low cost IC testing is now a burning issue in semiconductor technology. Conventional IC tester, ATE (automatic test equipment), cannot cope with the today's continuously increasing complexities in IC technology. Deterministic algorithm, which is an idea of 1960's, is adopted in the ATE. Recently pseudo-random testing approach has been emerged as an economically viable alternative to the expensive deterministic testing. This paper introduces a SOC implementing pseudo-random test technique for low cost IC testing with reliable performance. It is capable of testing combinational circuits as well as sequential circuits with scan-path facilities efficiently. It can also be used for testing PCB interconnection faults.

KEYWORDS: *ATE, Seed, LFSR, SOC.*

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INTRODUCTION

Dramatic improvement of integration technology in IC manufacturing is rapidly leading to exceedingly complex, multi-million transistor chips. All the functionalities of an electronic system are being integrated on a single chip in less than 2 cm square silicon area. This growth is expected to continue full force for the future years. With the increase of such integration densities and complexities, problems associated with testing of ICs have become much more complex and acute [1]. The cost of testing has become a major portion of the total cost of an electronic product. It is predicted in a survey that it will soon cost more to test a transistor than to make it if current trends of increasing testing cost is maintained [2]. IC testing has now become a front-end issue in semiconductor world, which needs an economic solution with reliable performance.

Modern IC manufacturing company uses ATE. The drawbacks of ATE are: (i) High equipment cost (ii) Slow test speed (iii) Huge memory requirements (iii) Tester inaccuracy. All the drawbacks of ATE are pointing towards having a new approach for cost effective IC testing. Otherwise all the benefits of semiconductor technology will be meaningless [3]. ATE is based on the deterministic algorithm. In deterministic approach [4], CUT is analyzed at the beginning of the test to generate pre-defined test patterns for detecting its faults. Deterministic test pattern enables error signals, generated due to presence of faults, and propagates them to some observable outputs from the faulty nodes or lines. This method guarantees full fault coverage but the increasing densities in the circuit leads to computational complexities and the requirements of huge amount of memory to store large test data volumes.

Pseudo-random approach [5] is now emerged as an economically viable alternative to the expensive deterministic testing. In this approach, a set of test vectors is generated randomly from 2^n possible input patterns (n= number of inputs). Linear feedback shift registers (LFSRs) are commonly used for test pattern generation because it has simple structure and can also be used as output response analyzer. The main advantage of this approach is that random pattern generation circuitry is simple and a large number of test pattern can be generated using smaller data storage.

The attempt to design and develop low cost IC tester is prevalent among the researchers since 1970. A small tester was built in the Laboratoire d'Automatique de Grenoble in 1970 and performed some random testing trials [6]. Test processor chip based on weighted random test techniques have been reported [7]. This paper introduces a SOC using pseudo-random test technique to develop a cost effective IC tester. The tester needs simpler hardware and control complexities and less memory space than that of others. Tester inaccuracy problem has also been addressed by introducing the concept of single chip IC tester which has been designed using industry standard HDL.

In order to maintain the accuracy of the tester, it is essential that the fabrication technology of the tester circuit should be at the leading edge with respect to the CUT. Since the design of the proposed SOC is in Verilog HDL, which is technology independent, the soft core can be reused to new fabrication technology keeping pace with the today's continuously changing technology environment. The performance of the IC tester has been verified using fault simulation technique. The following sections of this paper describe the design and operation of the SOC and fault simulation results of benchmark circuits.

DESIGN OF THE SOC

Figure 1 shows the functional block diagram of the SOC. Main modules of the SOC are a micro-UART, controller unit, test pattern generator (PG), buffer register (BR), signature analyzer (SA) and memory modules (RAMs). All the modules except memory modules have been designed using verilog HDL. The memory modules have been used from Altera Quartus library. The design has been compiled and simulated using the Qurtus EDA tool.

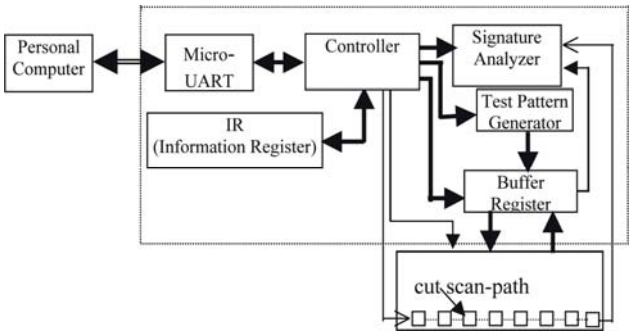

Fig. 1. Functional block diagram of the IC tester

DESCRIPTION OF THE MODULES

Micro-UART: It consists of a transmitter and a receiver module. Data communication between personal computer (PC) and the SOC is performed through the UART. It is named as micro-UART due to its modularity, configurability and extremely compact size [11]. A user friendly GUI as shown in the Figure 2 has been developed using C++ Builder for key-in test information such as numer of primary I/O, number of CUT scan-path, number of test set etc.

Controller: It consists of finite state machines (FSMs) and datapaths. FSMs generate sequence of necessary controlling pulses for loading data in the memory and executing the test process of the CUT.

Memory and Information Register (IR): Necessary information for testing CUT such as number of primary inputs, primary outputs, test set, test length etc. is stored in the IR and memory modules (RAMs). Three RAMs named as test length storage RAM (RAM_TL), seed stor-

age RAM (RAM_SD) for random pattern generation and signature storage RAM (RAM_SG) have been used.

Pattern Generator (PG**):** It is a 32 bit LFSR and its feedback connection is according to primitive polynomial $P(X) = 1 + X + X^{27} + X^{28} + X^{32}$.

Buffer register (BR): The BR is also 32 bit. Test pattern generated from the PG is loaded into the BR and is applied to the CUT and the output response is also captured into the BR and is sent to the SA.

Signature Analyzer (SA): The SA has similar structure of the PG except having two inputs. The state of the SA is given by the equation:

$S(t+1) = [T].[S(t)]^T + [R(t)]^T$ where, $S(t+1)$ and $S(t)$ are SA states at times t+1 and t respectively. [T] and $[R(t)]^T$ are the transition matrix of the SA and are the transition matrix of the SA and Aliasing error of the SA is $1/2^{32}$.

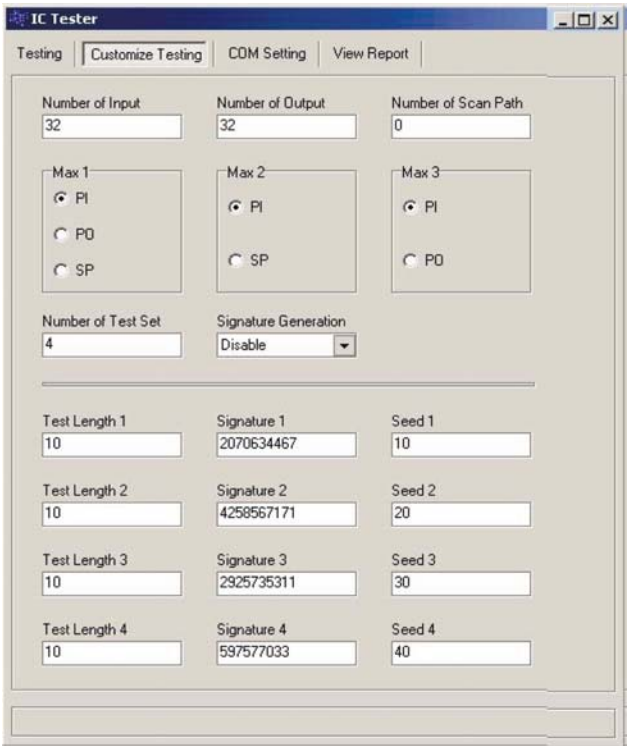

Fig. 2. Graphical user interface (GUI) between the SOC and the PC

OPERATION OF THE SOC

Operation of the SOC has two phases: (a) load/write data in the IR and the memory modules (b) circuit test and retrieval of test result. These two operations are controlled from the GUI as shown in the Figure 2.

Load/Write: Prior to IC testing, the following information is loaded in the IR and memory modules.

- Load the IR with necessary information such as number of CUT primary inputs and outputs, number of CUT scan paths, number of test sets,
- Load the test length of each test set in the test length storage RAM
- Load the data in the seed storage RAM for random test pattern generation
- Load the reference signature in the signature storage RAM.

Circuit test and response retrieval: At the beginning of test of IC, the PG, BR and SA are reset to zero and the test mode is set on from the GUI. The test sequences are as follows:

```
-----------------------------------------------------------------
Loop1
  If test mode on {
  Read the test length for the 1st test set,
  Read the seed value of LFSR for the 1st test set,
  Read the reference signature for the 1st test set,
  Set seed in LFSR by setting input set_seed=1,
  Loop2
  Enable LFSR for max(pi,sp) clock cycles,
  Enable buffer register for max (pi,po) clock cycles,
  Enable signature analyzer for max(pi,po,sp) clock
  cycles,
  Set the CUT to normal mode by setting input
  cnm=1 ;
  If cnm=1 {
    Apply test vector to the CUT
    Capture response and send to signature analyzer
    Increment test_counter value}
  If test_counter value=presetted test length {
          End_set(e_set)=1 ;
          Compare signature with reference signature }
Else goto Loop2
If e_set=1 {
          Increment set_counter, }
If set counter_value=presetted number of test set {
          End_test (e_test)=1,
          Ready for next test, }
}
Else goto Loop 1
-----------------------------------------------------------
```

SPECIFICATION OF THE SOC

Specifications of the SOC are as follows :

- Maximum CUT input/output pins: 32
- Maximum CUT scan-path: 128
- Maximum test: 4
- Maximum generated test vectors: 1.7×10^7
- Maximum test length 2^{14} K

FAULT SIMULATION RESULTS

For the evaluation of the performance of the IC tester, fault simualtion experiments on ISCAS85 benchmark circuits [9] have been conducted using TetraMax fault simulator of the Synopsis EDA tool. Pseudo-random testing approach has the drawbacks of requirements of higher number of test vectors to achieve acceptable fault coverage. This problem has been overcome by using appropriate seed of the LFSR.

Summary of the fault simulation results have been presented in the Table 1. It shows that if the LFSR is initialized using appropriate seed then it is capable of producing acceptable fault coverage using lower number of test vectors. The results are comparable with that of other researchers [7, 10].

Table 1

Summary of the fault simulation results

ISCAS85 Benchmark Circuits	Number of test vector	% Fault coverage
C432	288	100
C499	928	100
C880	384	98.74
C1355	1300	100
C1908	2208	100
C5315	1408	99.13
C6288	128	100

CONCLUSIONS

Design of a cost effective IC tester has been presented. Since the IC tester is SOC, it posses improved performance, improved reliability, reduced power consumption, reduced cost, reduced system size and short time-to-market. It requires lower data storage requirements. The performance of the tester verified and showed that it is capable of producing 100% fault coverage using lower number of test vectors.

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