A SERIES VOLTAGE REGULATOR INTEGRATED IN CMOS TECHNOLOGY

Helene Tap-Beteille, Marc Lescure,
Laboratoire d'electronique INP-ENSEEIHT, Toulouse, France,
tap@len7.enseeiht.fr

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ABSTRACT

Since the regulation of voltage supply is one of the most critical requirement of the electronic system design, the monolithic voltage regulator has become one of the most important building block of both analog and digital systems. This importance has been recently increased with the emergent low voltage technologies, encouraging industrials and researchers to work on new regulator structures. The voltage regulator presented here, has been first calculated and simulated through PSpice. The paper deals with the conception of a series voltage regulator integrated in 0.6Bμm CMOS technology. This type of regulators has become one of the most important building block of both analog and digital systems. It is constituted by a bandgap voltage reference and an error amplifier associated with a ballast element. The circuit obtained is unconditionally stable with good performances: a power-supply-rejection-ratio < 2%, an output resistance < 0.3 Ω and a temperature coefficient < 10 ppm. It is integrated on an ASIC for on board applications where low volume and low power consumption are key elements.

KEYWORDS: *Analog design, Bandgap circuit, CMOS technology, Integrated circuits, Voltage regulator.*

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INTRODUCTION

Since the regulation of voltage supply is one of the most critical requirement of the electronic system design, the monolithic voltage regulator has become one of the most important building block of both analog and digital systems. This importance has been recently increased with the emergent low voltage technologies, encouraging industrials and researchers to work on new regulator structures. The voltage regulator presented here, has been first calculated and simulated through PSpice. Then, the layout of the circuit has been drawn through Cadence Virtuoso and sent to foundry (0.6 µm CMOS technology).

We will first present the voltage regulators (section II). Then, we will present the bandgap voltage reference (section III) and the CMOS AOP circuit (section IV). To finish with, in section V, we will give the performances obtained.

THE VOLTAGE REGULATOR

The function of a voltage regulator is to provide a specified and constant output voltage from a fluctuating input voltage. The output voltage of this regulator (independent from the changing load conditions) would then be used to supply other circuits. Today, there are two different types of IC voltage regulators: the series regulators and the switching regulators [1]. The series regulator are connected in series with the load and the unregulated input voltage. They consist of three main elements as shown on figure 1. The voltage reference source generates a reference voltage Vr, independent of the unregulated input voltage variations or the temperature changes. The error amplifier compares Vr with a fraction of the output voltage Vo and generates a corrective error signal to regulate the voltage drop across the ballast element. Vo is derived from the actual output voltage by means of the sampling resistances R1 and R2.

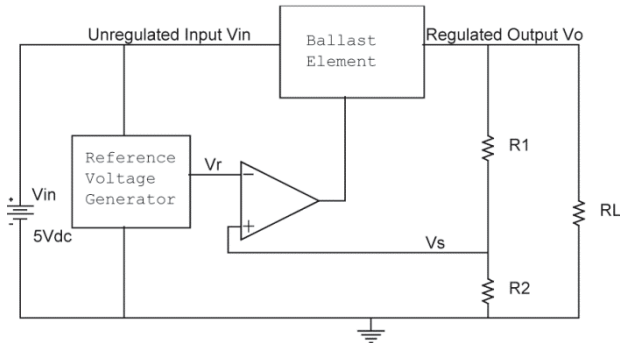

Fig. 1. Block diagram of series regulator

If the error amplifier gain Ad is sufficiently high, the voltage drop across the ballast element will vary with the fluctuations of the unregulated input voltage to maintain the output voltage V_0 constant and equal to:

$$V_o = \frac{A_d}{1+\alpha A_d} V_r \quad (1)$$

where α is the feedback factor, determined by the sampling resistances, that is:

$$\alpha = \frac{V_r}{V_0} = \frac{R_2}{R_1 + R_2} \quad (2)$$

Thus, the circuit produces an output voltage which is, to first order, independent of the input voltage and proportional to V_r. For most applications [2], the open-loop voltage gain A_d is on the order of 60-70 dB, which is usually obtained from two gain stages (a source-coupled pair and a common-source stage). That's why it has to be frequency-compensated to ensure stability under all operating conditions.

In CMOS technology, both MOS and/or bipolar transistor can be applied to generate the basic signals for voltage reference [4-6]. In case of MOS transistors, the basic signals are derived from the threshold voltage and the mobility. In the bipolar transistors, the base-emitter voltage and the saturation current are used for the extraction of the basic signals. It appears that the base-emitter voltage and saturation current of the bipolar transistors show better temperature characteristics than the threshold voltage and mobility of the MOS transistors. The low accuracy of the CMOS reference circuits is due to mismatching of components, drift, temperature effects, 1/f noise and mechanical stress. Thus, most of the voltage reference circuits apply bipolar transistors as the basic components [7]. That's why, we have integrated a bandgap reference, presented in next section.

THE BANDGAP REFERENCE

Figure 2 shows the implementation of the band-gap reference concept. The operational amplifier is in a feedback loop so the input differential voltage has to be a zero [3].

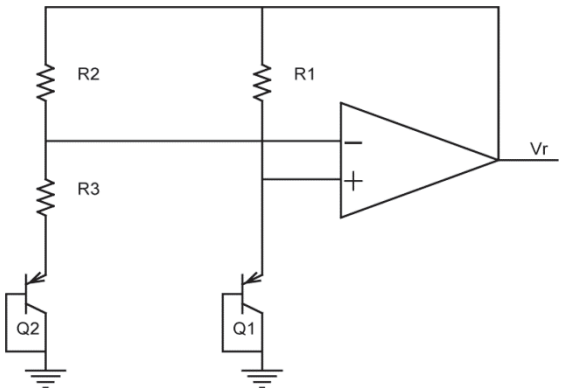

Fig. 2. Band-gap voltage reference circuit

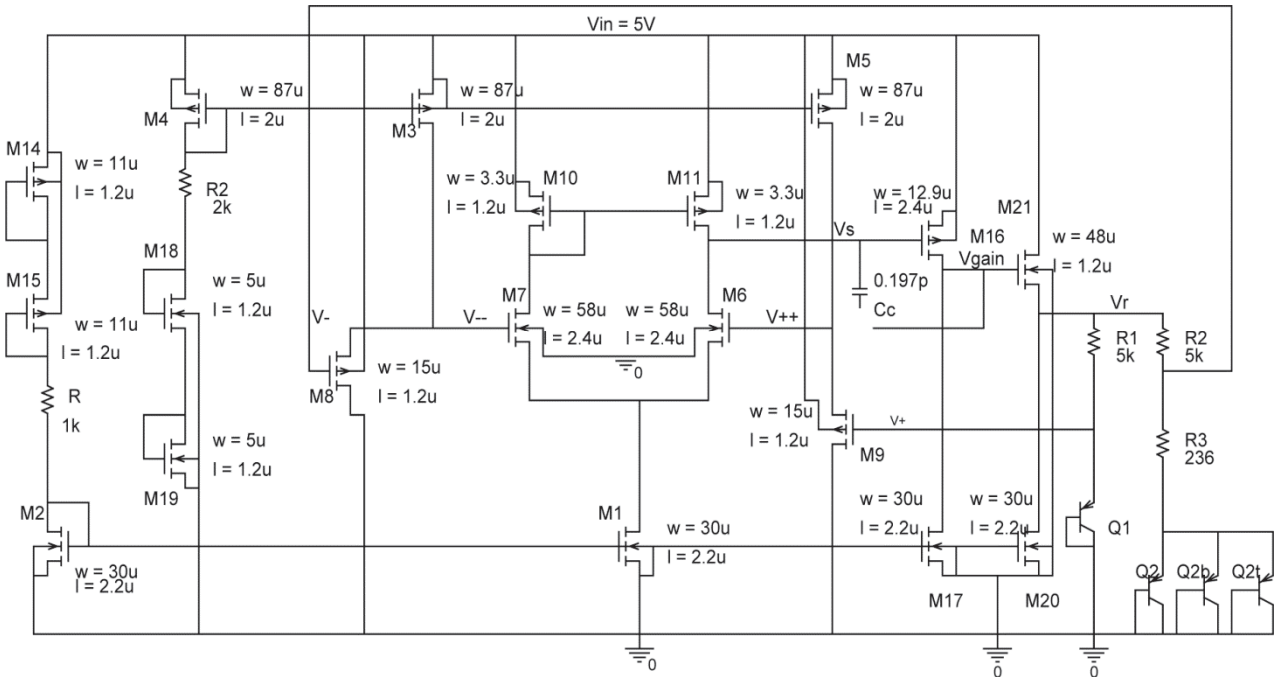

Fig. 3. Bandgap circuit

That's why I_1 and I_2 are forced to be equal to the ratio:

$$\frac{I_1}{I_2} = \frac{R_2}{R_1} \tag{3}$$

If Q_1 and Q_2 are well-matched and neglecting the base currents, the difference between their base-emitter voltages are:

$$V_{be1} - V_{be2} = \Delta V_{be} = U_T Ln\left(\frac{I_1 I_{s2}}{I_2 I_{s1}}\right) = U_T Ln\left(\frac{R_2 A_{E2}}{R_1 A_{E1}}\right) \tag{4}$$

With I_S = saturation current of the transistor, A_E = emitter surface of the transistor This differential voltage ΔV_{be} appears directly across resistance R_3, that is:

$$\Delta V_{be} = I_2 R_3 = \frac{I_1 R_1 R_3}{R_2} \tag{5}$$

That's why the reference voltage V_r is:

$$V_r = V_{be1} + R_1 I_1 = V_{be1} + U_T \frac{R_2}{R_3} Ln\frac{R_2 A_{E2}}{R_1 A_{E1}} = V_{be1} + K U_T \tag{6}$$

knowing that $\frac{\Delta V_{be}}{\Delta T} = -2\ mV/°C$ and

$\frac{\Delta U_T}{\Delta T} = +0.086\ mV/°C$, $K = -\frac{2}{0.086} = 23.3$

So V_r comes about +1.25V which is very nearly equal to the band-gap voltage of silicon.

The bandgap circuit is shown on figure 3. The gain of the differential stage is given by:

$$A_{diff} = \frac{V_s}{V^+ - V^-} = -\frac{g_{m6}}{g_{ds11} + g_{ds6}} = -158 = 44dB \tag{7}$$

with $g_m = transconductance = \sqrt{\frac{2 K_P W I_D}{L}}$ (8)

and $g_{ds} = \lambda I_D$ (9)

The gain of the second stage is given by:

$$A_{M16} = -\frac{g_{m16}}{g_{ds16} + g_{ds17}} = -47.9 = 34dB \tag{10}$$

So, the gain of the whole circuit is A_0 = 78dB. This two-stages amplifier is only marginally stable when used in a feedback circuit. So, we have to introduce a pole-splitting capacitance C_c to make the circuit always stable.

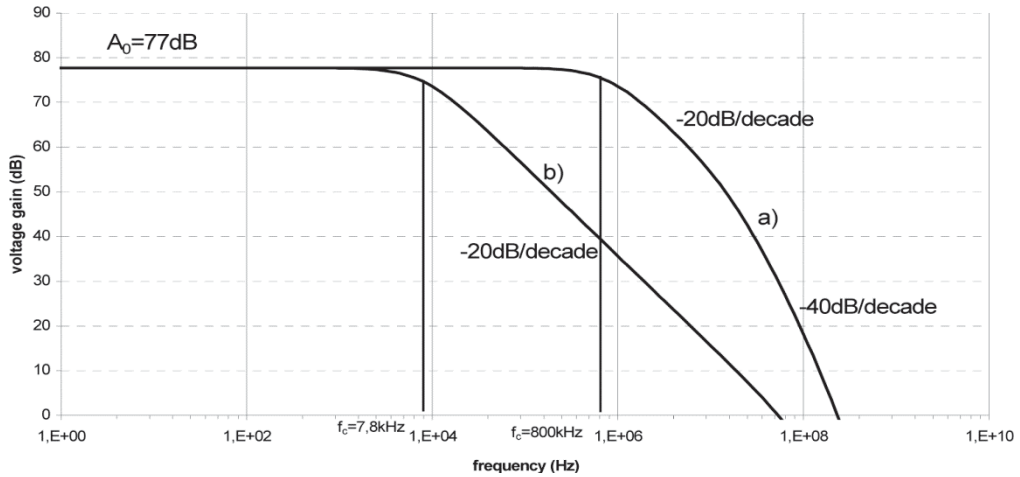

Fig. 4. a. Gain response without C_c; b. Gain response with C_c

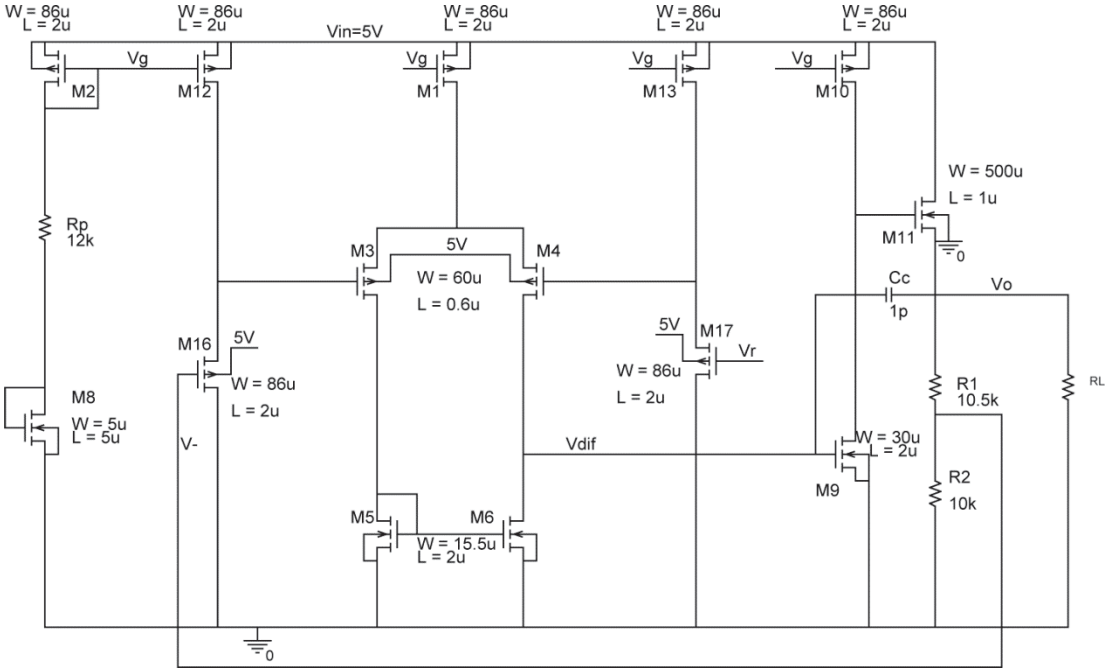

Fig. 5. Error amplifier and ballast element circuit

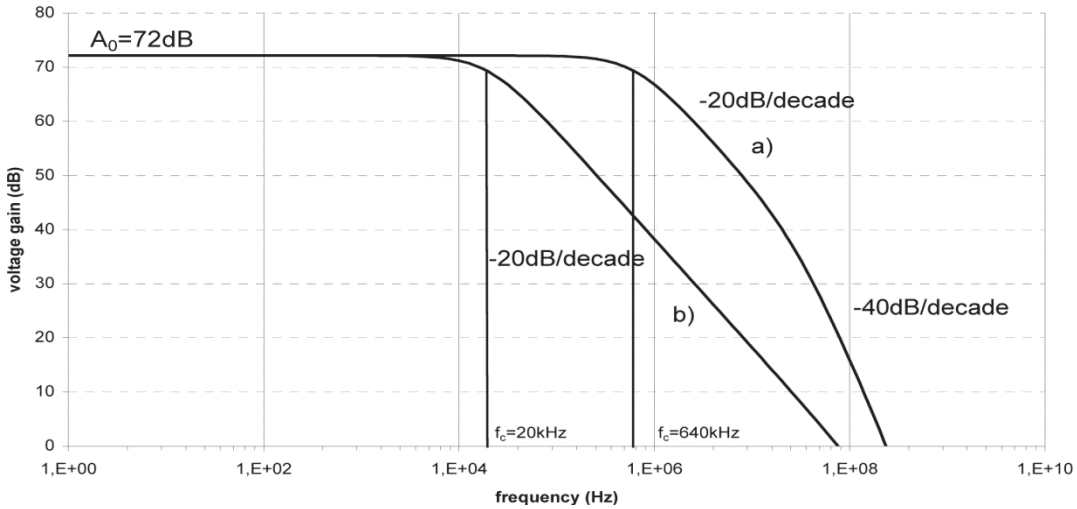

Fig. 6. a. Gain response without C_c; b. Gain response with C_c

The gain frequency response obtained with or without the compensation capacitance is shown on figure 4.

THE AOP AND THE BALLAST ELEMENT

The error amplifier and ballast element circuit is shown of figure 5.

The gain of the differential stage is given by:

$$A_{diff} = \frac{V_{diff}}{V^+ - V^-} = -\frac{g_{m4}}{g_{ds6} + g_{ds4}} = -35 = 31dB \quad (11)$$

The gain of the second stage is given by:

$$A_{M9} = -\frac{g_{m9}}{g_{ds9} + g_{ds10}} = -112 = 41\,dB \quad (12)$$

Neglecting the voltage gain of the source follower stages, the gain of the whole circuit is $A_0 = 72$ dB.

A pole-splitting capacitance C_c is used to make the circuit always stable.

The gain frequency response obtained with or without the compensation capacitance is shown on figure 6.

PERFORMANCES AND CONCLUSIONS

The temperature coefficient given by PSpice simulations is:

$$k_T = \frac{1}{V_0}\frac{\Delta V_0}{\Delta T} = 8\ ppm/^\circ C \quad (13)$$

The total power dissipation is 9mW. The global consumption without an external resistance load RL is 1.9mA. The power-supply-rejection-ratio is 1.4% and the output resistance is 0.025Ω.

So this paper shows that it is interesting to integrate a voltage regulator in a ASIC in order to regulate the input voltage of both analog and digital circuits, because the performances obtained are quite good for a reduced place. The circuit has been realised in CMOS 0.6µm technology.

This ASIC will be tested to compare the measured performances with the expected performances. If the measured performances are satisfying, the ASIC will be used in on board applications where low volume and low power consumption are key elements.

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