HIGH POWER AMPLIFIER PREDISTORTER ASIC IN STANDARD DIGITAL CMOS TECHNOLOGY

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ABSTRACT

Satellite communications offer a wide coverage for global communication systems. In order to increase spectral efficiency, non constant modulus constellations are very attractive compared to the classical BPSK and QPSK schemes. A 16-QAM modulation could offer a significant increase in spectral efficiency for satellite communications. Because the available power on board the satellite is strongly limited, High Power Amplifiers (HPA) like Travelling Wave Tubes (TWT) or Solid State Power Amplifiers (SSPA) are generally operated near the saturation point with a low back off. When operated with such low back off, HPA are highly non linear amplifiers. So, the signal to amplify being strongly distorted, a predistorter has been developed. A high power amplifier predistorter has been implemented in 0.6 m CMOS technology. First, the predistorter is briefly described. Then, the implementation of the predistorter is shown. The circuits designed for the neuron first layer are described, as well as the simulation results obtained.

KEYWORDS: *High power amplifier, MLP neural network predistorter, Gilbert cell, Kirshoff adder, analog circuits, 0.6 m CMOS technology.*

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PREDISTORTER DESCRIPTION

The predistorter must fight against two impairments given by the non linear amplifier, the AM/AM and AM/PM conversions. In order to do that, a mimic structure has been adopted [1], [2]. The predistorter is composed of two Neural Networks (NN), one NN computes the phase shift correction and the other one computes the gain correction. The input of both NN is the square modulus, $\rho^2 = I^2 + Q^2$, of the input signal I+jQ. Data I and Q having a 25MHz bandwidth, the input of the NN, ρ^2, is a 50MHz signal. All details concerning the structure of the predistorter can be found in [4] for example. Each NN is a MLP network with 10 neurons in the hidden layer. The architecture of one of the NN is shown on figure 1.

W1k and b1k are respectively the input weight and bias (or offset) of the first layer of neuron number k. W2k is the output weight (or gain) of neuron k, while f(.) is a non linear function like a hyperbolic tangent function. b2 is the output bias of layer 2. The weights and biases are updated following a gradient based algorithm using back propagation [3].

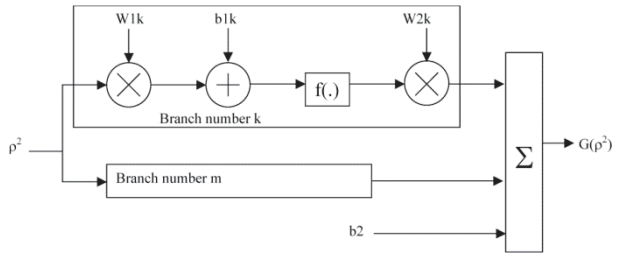

Fig. 1. Architecture of the MLP Neural Network

PREDISTORTER IMPLEMENTATION

The NN core is implemented in an analog ASIC whereas the adaptive algorithm is implemented in an external DSP. For the digitization of signals, 8 bits DAC converters are sufficient. This technique is particularly attractive because of the high integration density for the NN core; the good accuracy and the easy memorization for the algorithm part. Moreover, analog implementation permits to control high frequency signals unlike digital techniques; and implementing the algorithm on a DSP permits the future evolution of the adaptive algorithm.

The NN core is realized with a submicronic CMOS technology because CMOS offers a good reliability as well as reproducibility. The maximal bandwidth and the power supply are determined by the minimum length of the transistors channel. So, we have first verified that the circuits bandwidth was sufficiently high in 0.6 µm technology (> 50MHz) [4]. This technology permits to use a 5V power supply instead of 3.3V for a 0.35 µm technology. Having a higher voltage permits to have a higher dynamic range of the neuronal functions. The choice of the packaging is made by computing the number of inputs/outputs, considering the neural network, one test neuron, test elementary cells and more than 10 ground pins evenly distributed. This balance sheet, reported on table, imposes to use a JLCC84 case.

Table 1

Balance sheet of the 84 pins ASIC

function	Pin names	mode	quantity
square modulus ρ^2	I and Q	input	8
square modulus ρ^2	ρ^2	output	1
Neuron first layer	ρ^2	input	1
Neuron first layer	First weight W1	input	10
Neuron first layer	First bias b1	input	10
Hyperbolic tangent function	Tanh output	output	10
Neuron second layer	Second weightW2	input	10
Neuron second layer	Second bias b2	input	1
Neuron second layer	Predistorter output	output	1
Test branch	/	/	7
Test cells	/	/	13
Electrical ground	/	/	12
			Total 84

To implement the neuronal functions, three types of analog cells are necessary [5]: adders, four-quadrant multipliers and a non linear function. Many possibilities have been explored to realize these functions. At last, all the functions implemented on the ASIC are Gilbert cells, Kirshoff adders and sources-coupled differential cell to realize the hyperbolic tangent function. Each cell has been individually optimized depending on its specifications and place in the predistorter.

THE SQUARE MODULUS FUNCTION ρ^2

The implementation of the square modulus function is shown on figure 2. It is composed of 2 Gilbert cells configured like frequency doublers, to perform I^2 and Q^2 respectively. A Kirshoff adder is used to perform $I^2 + Q^2$.

The maximum dynamics of the input signals(I(t) and $Q(t)$) has been evaluated, in order to reduce noise while preserving a signal distorsion < 1% at the output of the function. The maximum amplitude of the differential input voltage $\Delta V_{d\ Max}$ allowed for I and Q signals in order to avoid the saturation of the output differential current is [6]:

$$\Delta V_{d\,Max} < \sqrt{\frac{I_{pol}}{K_P (W/L)}} \cong 250\,mV \qquad (1)$$

Ipol = 500 µA +/- 20%, the current supplied by Q7 or Q'7, K_p = µon C_{ox} = 120e^{-6} A^2/V +/-20%, W/L = 40µm / 0.6µm the channel size of the sources-coupled pair.

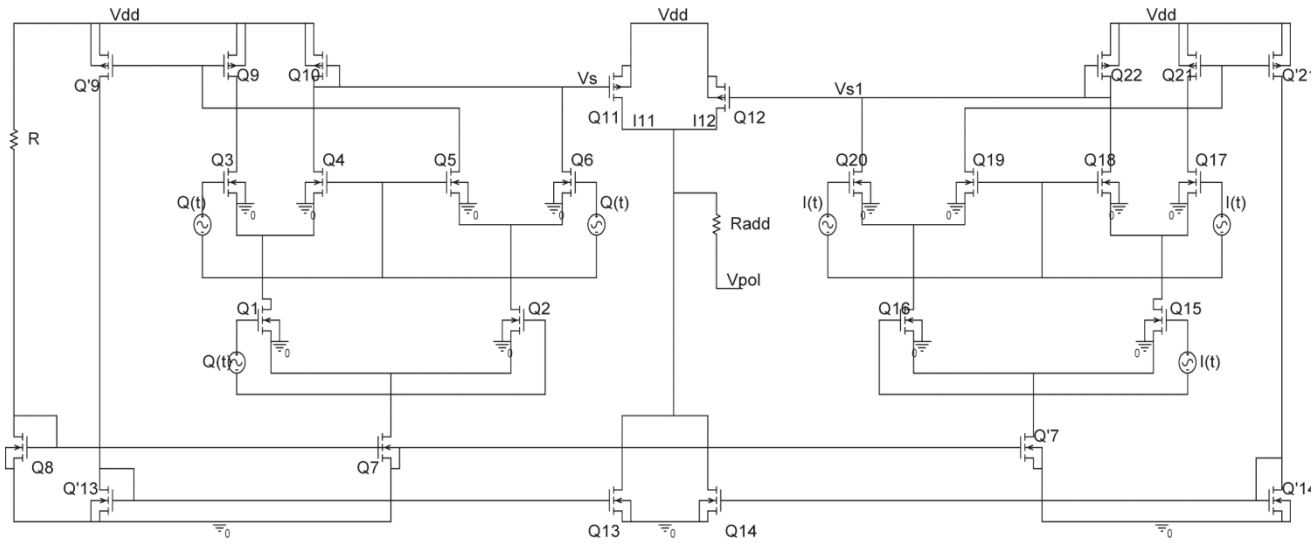

Fig. 2. The square modulus function is composed of 2 Gilbert cells and a Kirshoff adder

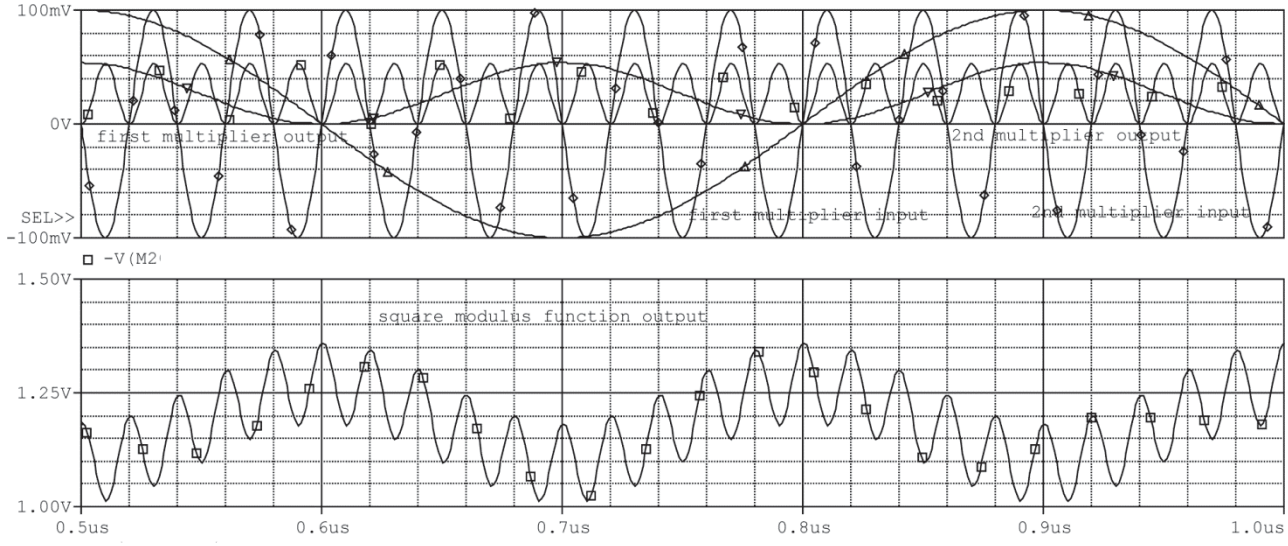

Fig. 3. a) ◇ first multiplier input, □ first multiplier output, Δ second multiplier input, ▽ second multiplier output;
b) □ square modulus function output

I_{pol} is not very well known because of the absolute tolerance on the sheet resistances, as well as K_p. That is why we have chosen I and Q range around 200mV to stay in the linear region of the transfert of the differential pairs as well as being strongly superior to the voltage noise. Simulation results showing the multipliers outputs and the function output are reported on figure 3.

THE NEURON FIRST LAYER

In the neuron first layer (fig. 1), there is to multiply the square modulus with a weight (to control the amplitude and the polarity of the signal) and to add it a bias (to control the d.c.value). Both functions have been implemented together as shown on figure 4.

The output of the square modulus function is applied on the gate of Q3 and Q4 through the use of an external capacitor in order to filter the d.c.value of ρ2. Matlab simulations have shown that the high-pass filter obtained must have a low cutoff frequency less than or equal to 1MHz to keep a Signal to Error Ratio of 36dB [7]. SER being the ratio between the HPA output power and the power of the identification error. Knowing that the input resistance R = 10kΩ, the external capacitor C must be equal to or higher than 16pF.

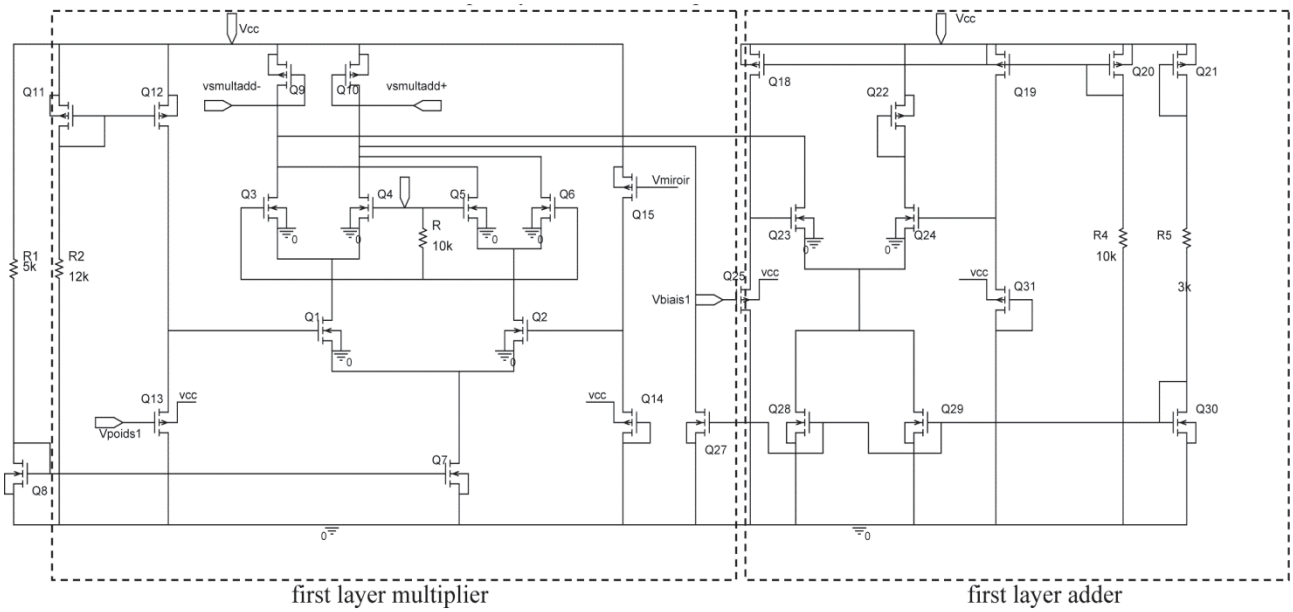

Fig. 4. Neuron first layer: the square modulus function output is multiplied with a weight called "vpoids1" and is added with an offset called "vbiais1"

This value is too high to be integrated in the ASIC, that is why the connection between the output of the square modulus function and the input of the neuron first layer is external. The multiplier used is a Gilbert cell where the signals to multiply are the output of the square modulus function and the weight called Vpoids1.

The principle of the adder part is to create a current I in Q30 which is mirrored in Q27, Q28, Q29. Q27 will always impose a current I to one of the cell outputs (Vsmultadd+). A current 2I must be provided by Q23 + Q24. Each of them will provide a current I when Vbiais1 = 0. So, Q29 will impose a current I to one of the outputs of the multiplier, as well as Q27 to the other output. In this case the d.c.value of the cell output (Vsmultadd+ - Vsmultadd-) is equal to zero.

If Vbiais1 increases, current in Q23 increases, so the d.c. value of (Vsmultadd+ - Vsmultadd-) increases ; and conversely. The output of the cell (Vsmultadd+ - Vsmultadd-) is presented on figure 5a with vbiais1 = 0V and Vpoids1 varying between –0.5V and +0.5V and on figure 5b with Vpoids1 = 0.1V and Vbiais1 varying between –0.5V and 0.5V. The input of the cell is a 50MHz sine.

Then, the output signal is multiplied with a tanh function (fig.1). The function has been realized with a source-coupled differential pair [4].

Figure 6 represents both drain currents versus the input differential voltage (curve a). The hyperbolic tangent function has also been plotted (curve b).

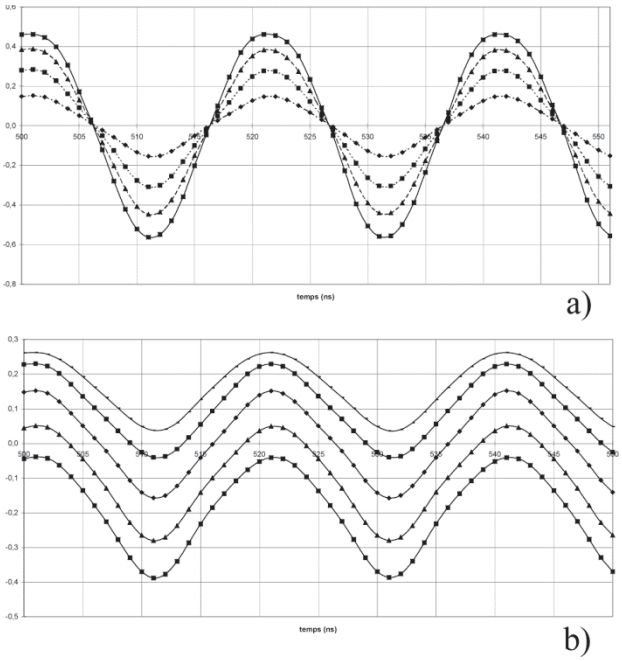

Fig. 5. Output of the first layer multiplier-adder (Vsmultadd+ - Vsmultadd-):
a) vbiais1 = 0V, -0.5V<Vpoids1<0.5V;
b) vpoids1 = 0 V, -0.5V<Vbiais1<0.5V

The neuron second layer, as well as the output adder, consists of the same functions as those constituting the first layer.

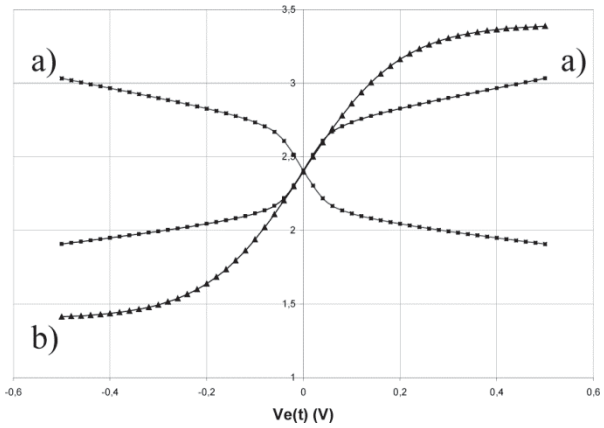

Fig. 6. a) drain currents of the source-coupled differential pair (simulation results); b) hyperbolic tangent function

CONCLUSIONS

We have simulated a Neural Network predistorter. This NN is based on a MLP structure. Because of the high speed of the transmitted signal (higher than 25MHz), we have adopted an analog implementation of the MLP Neural Network. The circuit has been implemented in 0.6µm CMOS technology.

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