EFFICIENCY ANALYSIS OF SWITCHING CONVERTER-MODULATOR

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ABSTRACT

The article discusses methods of highly efficient linear RF power amplifier and transmitter design for future 5G/6G networks. Based on a consideration of various known methods for constructing high-efficiency power amplifiers, the prospects of developments using the envelope elimination and restoration (EER, or Kahn method) and envelope tracking (ET) method are substantiated. The prospects for implementing PWM switching converter-modulator for these methods are assessed. Based on the evaluation calculations performed, it is shown that this structure can potentially be used as an EEP/ET modulator for a number of 5G/6G applications and will have advantages over structures using class AB amplification.

KEYWORDS: *Envelope elimination and restoration, Envelope tracking, High efficiency RF power amplifier, PWM Modulator.*

1 Introduction

Linear RF power amplifier (PA) and transmitter design is a large and extremely active research area for a wide range of applications in mobile and fixed radio technology, especially for future 5G/6G networks [1]. A number of linear transmitter techniques are available for commercial exploitation, with others at varying degrees of development [2, 3]. Therefore, it is possible to implement with current technology, many of degrees of freedom required in a flexible transmitter (for example, in terms of channel bandwidth, frequency coverage and required distortion performance). It is not possible yet to cover all of these requirements in a single, high-efficiency design.

The most popular techniques of PA's efficiency improvement are:

• Digital PA [4];
• Doherty system;
• Chireix – outphasing system [5];
• Polar modulation (Kahn – EER (envelope elimination and restoration) system) [6];
• Dynamic power supply voltage (envelope tracking – ET) [7-9];
• Dynamic current control (dynamic bias control);
• Hybrid methods [10-16].

Part 2 of this work describes the general characteristics of the methods presented above. It is shown that methods such as EER and ET with a switching mode PWM modulator can become most widespread for future applications. Part 3 provides a preliminary evaluation of the effectiveness of their use for the design of 5G/6G PA. Conclusions on the work are made in part 4.

2 Power Amplifier's Efficiency Improvement Methods

Digital PA consists of many elementary switching RF PAs that operate in classes D, E or F [4]. Its advantage (theoretically 100% DC to RF power conversion efficiency at all signal levels) can be realized in high power levels only (hundreds of W or kW approximately). Linearity of this technique decreases with back-off. A digital PA used in high power broadcast AM/DRM (Digital Radio Mondiale) transmitters with peak-to-average ratio of output power from 6 to 10 dB, and back-off below 6-9 dB.

Doherty system and Chireix – outphasing system (classical) offer improved average efficiency, but only over a limited range of back-off [19, 20] (Fig.1). These techniques were also common in high-power AM broadcast transmitters. They are being actively researched at present, but are not very suitable for wideband applications - both in terms of operating frequency and the width of modulating frequencies.

Chireix – outphasing system can used with Power Re-Use (recuperation) Technique (in microwave PAs) for improved efficiency at low output power levels (at 10 dB of back-off additionally) [21]. The lack of more widespread use can be attributed to its greater complexity and the need to employ different transmitter architecture. This technique can be analized in the future work.

The use of high-efficiency switching amplifiers again results in the potential of achieving 100% DC to RF power conversion efficiency and this is a major attraction of the technique. There are, however, a number of problems. First, the requirement for a cancellation process at the output of the transmitter results in stringent control requirements for the gain and phase matching of the two RF paths. This is one of the problems, which feedback mechanism employed in the CALLUM technique attempts to solve [22].

Secondly, the cancellation process itself, occurring as it does at the output of the amplifier, results in a potential loss of efficiency of up to 50%. This occurs if a hybrid power combiner is used in the summation process, as the cancelled power is then wasted in the 50 Ohm load connected to the difference port. The amount of power wasted will depend upon the modulation scheme in question, but this is still a significant problem with the technique.

Studying of the PAs with 80% efficiency shows that the resulting efficiency at the low power signal levels is similar to the same in class A. Let us have two channel amplifiers with the output power levels 0,25W (0,5W) and 80% efficiency for each of them. So, the power consumption will be 0,625W. Overall efficiency in this case will be 0,16% for 1mW output. The recuperation technique with 50% efficiency will increase the overall efficiency twice of previous example (0,32%).

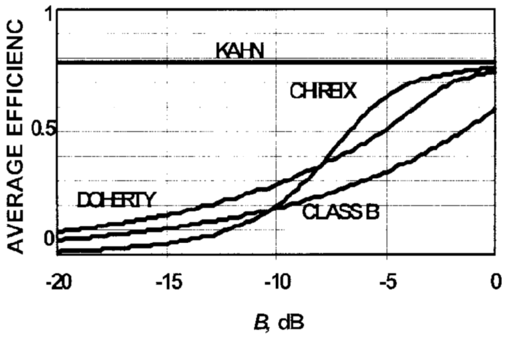

Fig. 1. Average efficiency of ideal PAs in back-off [23].

Kahn – EER system transmitter [6] operates with high efficiency over a wide dynamic range and, therefore, produces a high average efficiency for a wide range of signals and power back-off levels [23]. In either guise it has the potential, theoretically at least, to achieve 100% DC to RF power conversion efficiency at all envelope levels of the modulation signal.

The potential for high levels of efficiency stems from the fact that the RF power amplifier is freed from the requirement to amplify envelope varying signals and thus can be implemented by one of the switching RF power amplifier classes (e.g. class-D, E or F). Similarly the 'audio frequencies' (AF) envelope amplifier, which is effectively supplying the 'DC' power to the RF amplifier (and thereby applying high-level amplitude modulation), can be implemented by a switching audio amplifier technique (e.g. pulse-width modulation (PWM), class-S). As both of these types of amplifier are theoretically 100% efficient, and as there are (ideally) no other loss mechanisms (e.g. couplers or delay-lines) in the high-power RF path, the overall amplifier could be 100% efficient. Clearly a practical realisation will fall short of this goal, but a 20% implementation margin (in efficiency terms) would still result in an 80% efficient linear amplifier – a highly-desirable result.

Practical EER transmitters have been built for a number of applications, however there are a lot of practical problems which limit, in particular, the linearity available from the system. The use of high-level modulation of the power supply is not a particularly linear method of modulating an RF carrier, especially at low envelope levels (and power back-off), where the RF power transistor will cut-off introducing significant distortion. Furthermore, the switching frequency of the AF PWM amplifier must be at least 5…10 times exceeding of the RF signal bandwidth. With 5 MHz signal bandwidth the switching frequency of AF amplifier must be greater than 50 MHz. This is the very difficult task to solve it with high efficiency.

However, this technique has got a high potential for 5G/6G systems and will be studied in the future. Estimation of an opportunity of realization switching DC-DC converter on high frequencies will present at ch. 3.

Dynamic power supply voltage (envelope tracking) system has theoretical efficiency less than the EER systems but provides a good linearity at all power levels because of RF PA capability to operate in AB class. In this case, an AF amplifier is less difficult to realize than EER because its amplitude variation is smaller. There are still problems with signal filtering due to the harmonics of the AF amplifier. An example of efficiency improvement for this technique is presented in Figure 2 [24].

It can be proposed slow supply voltage control in tie with output power level. This approach results in efficiency decreasing (it still higher than the same in A or AB classes) but also gives significant simplification of an AF amplifier design, what can be explained by fact that bandwidth of amplifier will be defined by the rate of output power switching.

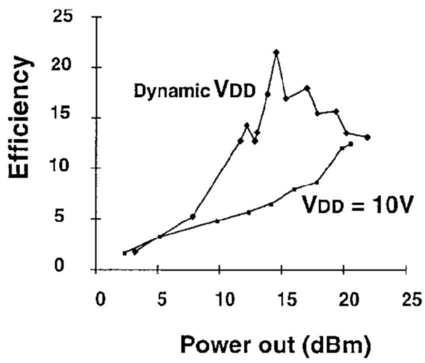

Fig. 2. Measured efficiency versus output power for dynamic supply amplifier and for a comparable amplifier with fixed VDD [24].

Dynamic current control (dynamic bias control)

This method has the lowest efficiency of previous studying, but is ease of design. Low power of controlling signals gives possibility to realize this structure in a single PA IC. The simplest application of this method is the bias current switching at low power operations (low power mode). This application has been realized in some of the modern PA ICs. This resulted in efficiency increasing of about 7% at P_{out} = 16dBm.

3 Estimation of an opportunity of realization switching DC-DC converter on high frequencies

Switching regulators and modulators based on Pulse Width Modulation (PWM) find wide application in engineering of the communications due to their high efficiency. Clock frequencies of produced and developed similar devices usually do not exceed 0.4 … 3.0 MHz. At such low clock frequencies the output filter should have big inductances (about few uH) and capacitors (about few uF) with large PCB area.

There are known switching DC-DC converters without use inductance based on overcharge of capacitors (charge pump). However similar devices have high output impedance and consequently work with small output current.

In the present section it will be carried out the theoretical researches of influence of the basic parameters of MOS transistors and clock frequency on PWM modulator efficiency.

Statement of a task.

The analysis will be made using the block diagram shown on a Figure 3, which represents the synchronous converter on complementary MOS transistors. The basic losses in such structure are commutative (switching) loss P_{com} on overcharge of transistor capacities and loss in resistors Ron of open transistors.

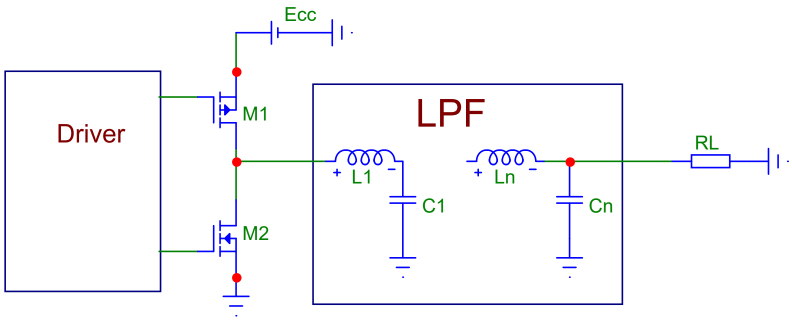

Fig. 3. DC-DC with PWM

Commutative loss of two transistors M1 and M2 at a rectangular drive voltage swing from 0 to Ecc on each gate and drain of transistors is defined by his total capacity (input and output), clock frequency *Fo* and input voltage *Ecc*:

$$P_{comm} = F_0 * C * E_{cc}^2 .$$

Losses on resistors of open transistors *Ron*, in the assumption, that they are equal, are defined by the following expression:

$$P_R = I_L^2 * R_{on} = P_{out} * (R_L + R_{on} / R_L) \text{, where:}$$

I_L - constant current in load R_L;

$P_{out} = U_L^2 * R_L$ – output power of DC current in load R_L.

The maximum available efficiency of the output stage is defined by the ratio of output P_{out} and consumed *Po* powers:

$$\eta = P_{out} / P_0 = P_{out} / (P_{out} + P_{com} + P_R) .$$

The simulation results of DC efficiency vs Pout are given on the diagrams of a Figures 4-7. On Figures 5-7 total capacity C=900 pF corresponds to power MOS transistors (similar to IRFZ24N, IRF9Z24N with C=900pF; Ron=0.1 Ohm), and total capacity C=200 pF corresponds new technologies with C=200pF; Ron=0.1 Ohm.

Similar dependences of efficiency for linear regulator of a compensation type (Lin DC-DC), calculated based on following expression:

$$\eta_{LIN} = P_{out} / P_0 = \sqrt{(P_{out} * R_L)} / E_{CC} .$$

In both cases the maximal DC output voltage on load R_L is defined by:

$$U_{L\max} = E_{CC} * (R_L + R_{on} / R_L) .$$

It is important to note, that except for the losses, considered above of lowering efficiency, there are also others losses with which it is possible to struggle technological and circuit technique methods.

One of such reason is through current proceeding through transistors, if his both are open or in active mode. For prevention of this effect it is necessary to design the driver so that between unlocking pulses on gates of MOS transistors there was a small time interval.

The second reason of additional losses is the internal resistance (R_G) in a gate circuit of the MOS transistors, which together with input capacity C_{GS} forms integrating *RC* circuit. This circuit increases times of front and recession of pulses drain current, during which the transistors work in active mode, that also results in efficiency decrease. According to said above special attention by transistors selection should be paid to low value of R_G.

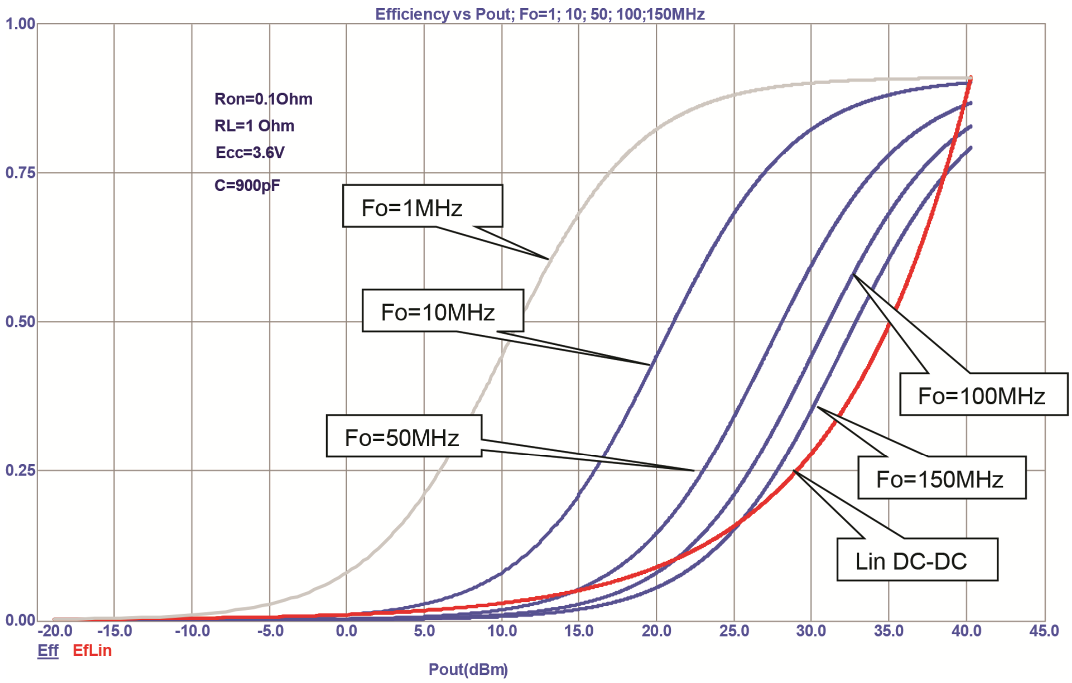

Fig. 4. Dependence of efficiency linear (red line) and PWM modulator (blue lines) vs output DC power (dBm) at various PWM clock frequencies: F_0=1; 10; 50; 100; 150 MHz. (Power MOS transistors similar to IRFZ24N, IRF9Z24N with C=900pF; R_{on}=0.1 Ohm) and R_L =1 Ohm; E_{cc}=3.6V.

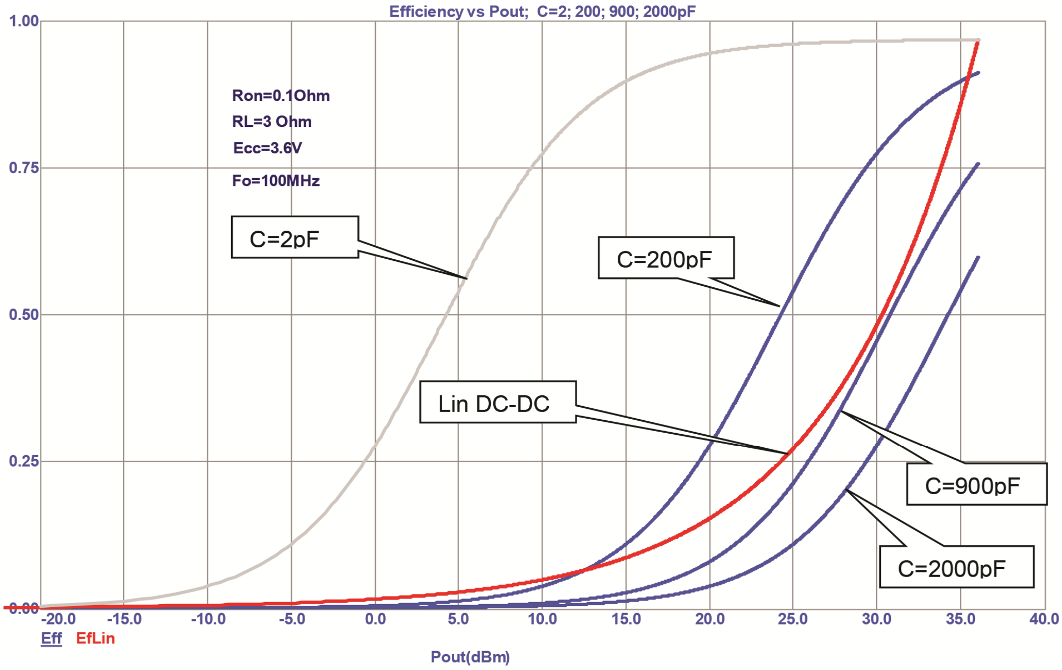

Fig. 5. Dependence of efficiency linear (red line) and PWM modulator (blue lines) vs output DC power (dBm) at various capacities of PWM transistors: C=2; 200; 900; 2000; pF. F_0=100 MHz; R_{on}=0.1 Ohm; R_L =3 Ohm; E_{cc}=3.6V.

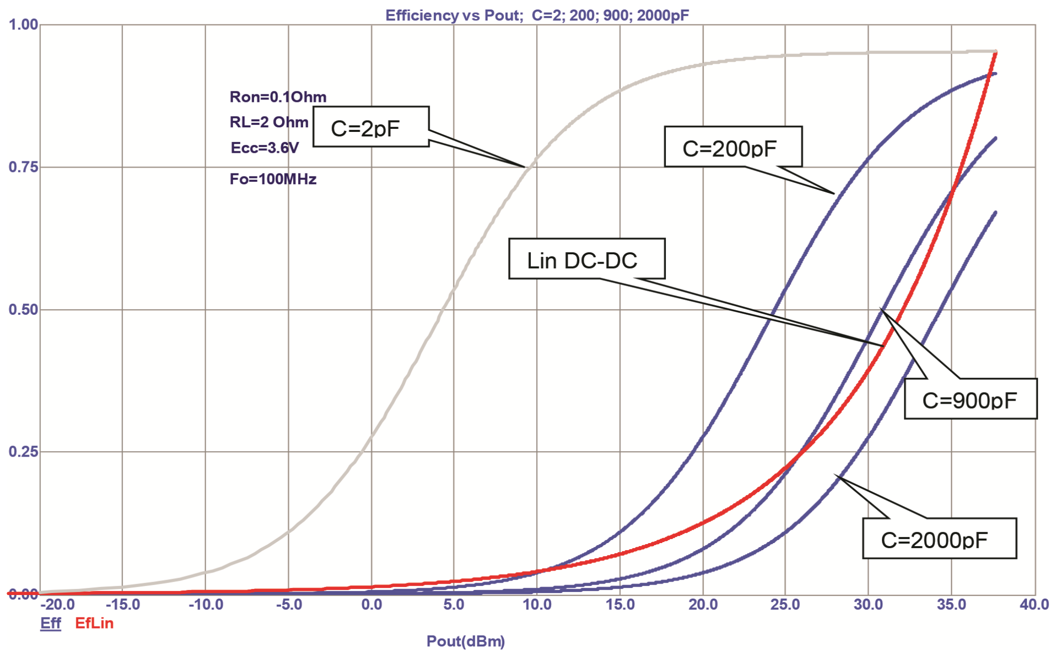

Fig. 6. Dependence of efficiency linear (red line) and PWM modulator (blue lines) vs output DC power (dBm) at various capacities of PWM transistors: C=2; 200; 900; 2000; pF. F_0=100 MHz; R_{on}=0.1 Ohm; R_L =2 Ohm; E_{cc}=3.6V.

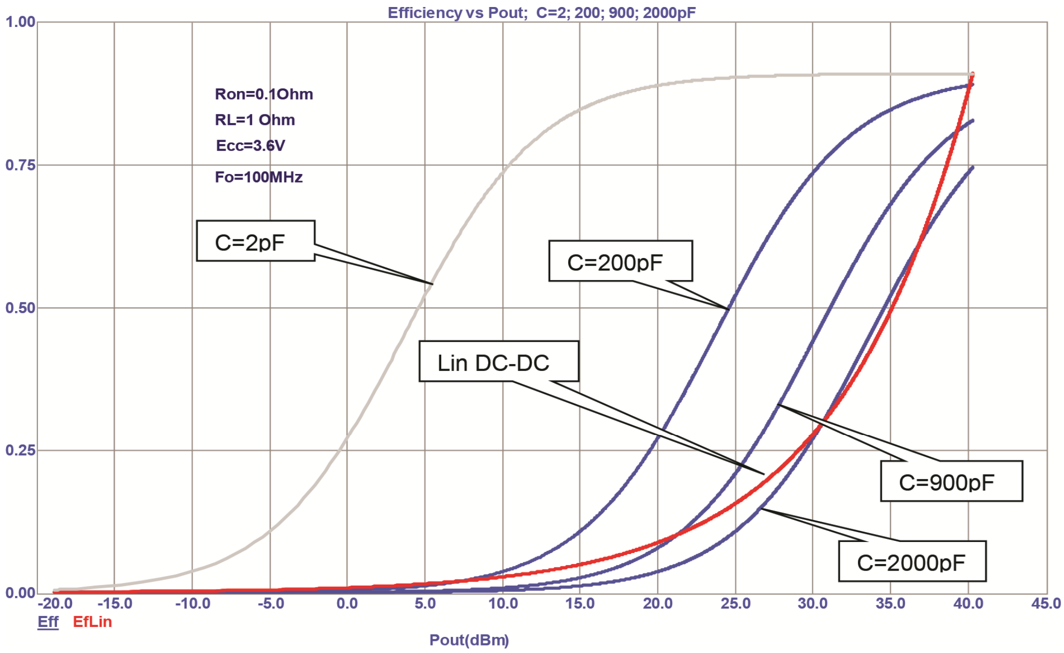

Fig. 7. Dependence of efficiency linear (red line) and PWM modulator (blue lines) vs output DC power (dBm) at various capacities of PWM transistors: C=2; 200; 900; 2000; pF. F_0=100 MHz; R_{on}=0.1 Ohm; R_L =1 Ohm; E_{cc}=3.6V.

From the results given above follows, that the basic reason of efficiency decrease in PWM modulator on high clock frequencies are the capacities of transistors.

However with total capacity of transistors pair C = 200 pF the limiting efficiency of the PWM modulator on frequencies $F_o \approx$ 100 MHz are higher than at the linear modulator at output power range from ≈10 mW to 5…10 W with load from 1 to 3 Ohm.

This structure can potentially be used as an EEP/ET modulator for a number of 5G/6G applications.

4 Conclusion

- Methods fo improving the energy efficiency of 5G/6G PA are considered.
- An assessment of the feasibility of implementing a DC-DC switching converter at high frequencies has been developed. This structure can potentially be used as an EEP/ET modulator for a number of 5G/6G applications.

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