SYNCHROINFO JOURNAL

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PHASE SHIFTERS AND ATTENUATORS IMPLEMENTATION FOR ACTIVE TRANSMITTER SIGNAL CANCELLATION IN THE RECEIVING PATH FOR SDR

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ABSTRACT

Many wideband duplex SDR applications do not use a receiver (RX) bandpass filter, so the low-noise amplifier (LNA) in the receive path must have a higher dynamic range, which comes with an increase in power consumption. To solve this problem, active transmitter signal cancellation in the receive path is used. These capabilities are considered for 5G New Radio Wireless Transceivers, for Multiple Input Multiple Output (MIMO) systems and radar applications. Solutions for the implementation of individual units, such as a delay line, digital applications, including in conjunction with analog, for various radio wave propagation channels and using neural networks are actively considered in modern literature. This paper considers options for implementing phase shifters and attenuators required for this device. The simulation of the considered implementation options for phase shifters and attenuators examples showed that the resistive digital step attenuator with a switch on MOSFETs and the attenuator on P-I-N diodes are not recommended for implementing the attenuator and phase shifter blocks of the compensation circuit. Active digital step MOS attenuator based on weighted current summation has a good dynamic range, but the output noise level seems too high over the entire possible current range. Therefore, this circuit needs noise optimization to be proposed for practical implementation. Active digital step MOS attenuator based on the composition of weighted current sources has intermodulation distortions less than –40 dB, a small parasitic phase shift and a low noise level. The high dynamic range allows installing a fixed attenuator and further reducing the output noise.

KEYWORDS: *SDR, phased antenna arrays, software-defined radio systems, Multiple Input Multiple Output, phase shifters, attenuators*

DOI: 10.36724/2664-066X-2024-10-4-2-13

Received: 12.06.2024
Accepted: 20.07.2024

Citation: Oleg Varlamov, "Phase shifters and attenuators implementation for active transmitter signal cancellation in the receiving path for SDR" *Synchroinfo Journal* **2024**, vol. 10, no. 4, pp. 2-13

1 Introduction

Phase shifters and controlled attenuators are actively used in a large number of devices from HF to microwave frequency ranges. Traditionally, controlled attenuators were used as gain control elements of receiving paths, including at the input of the device to avoid its overload with powerful signals. Currently, phase shifters and controlled attenuators are widely used in the electronic formation of phased antenna arrays (PAA) radiation patterns, determining the direction of electromagnetic radiation sources (radio direction finding), as well as in the circuitry of active transmitter signal cancellation in the receiving path for software-defined radio systems (SDR).

Since many wideband duplex SDR applications do not use a receiver (RX) bandpass filter, the low-noise amplifier (LNA) of the receive path must have a larger dynamic range, which is accompanied by an increase in power consumption. To solve this problem, active transmitter signal cancellation in the receive path is used [1, 2]. These capabilities are considered for 5G New Radio Wireless Transceivers [3], for Multiple Input Multiple Output (MIMO) systems [4] and radar applications [5]. Solutions for the implementation of individual nodes, such as a delay line, are considered in [6]. Digital applications are studied in [7-9], including jointly with analog [10], for various distribution radio wave propagation channels [11] and using neural networks [12]. Some options for active transmitter signal cancellation in the receiving path for SDR are considered by the authors in [13]. In this paper, the options for implementing phase shifters and attenuators necessary for this device are considered.

2 Phase Shifter

One of the best ways to organize the phase shift with additional attenuation can be the use of simple programmable attenuators in the signal channels with a phase shift of 90 degrees between them, as shown in Figure 1. To ensure good phase matching, all 4 programmable attenuators must be matched with each other. To reduce the number of attenuators, the following can be proposed: the phase shift is performed for the signal from one end, and the final conversion to the differential interface is performed inside an additional phase splitter, as shown in Figure 2.

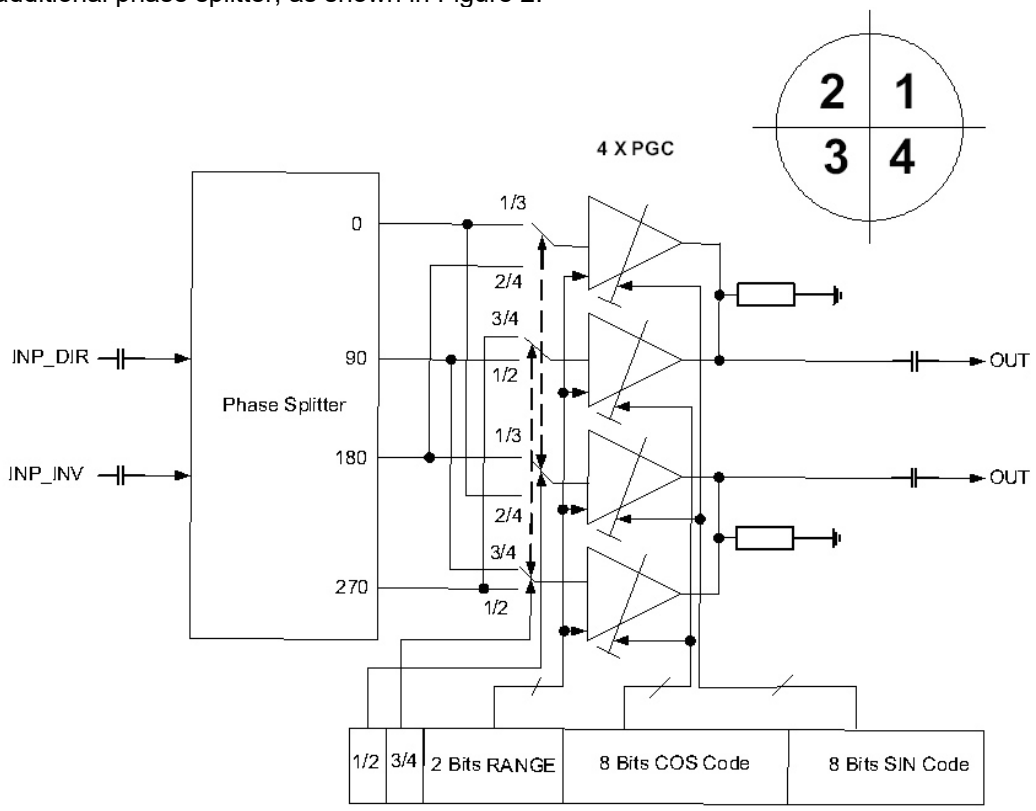


Fig. 1. Implementation of a phase shifter with 4 attenuators

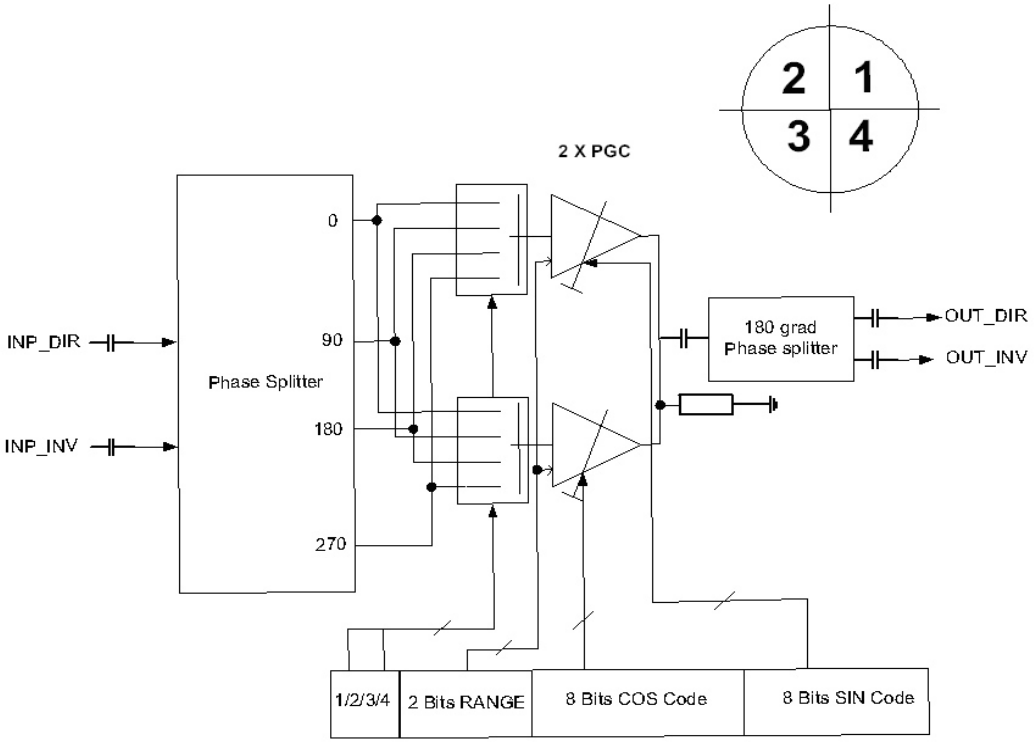


Fig. 2. Implementation of a phase shifter with 2 attenuators and a phase splitter

In the latter case, two attenuators can be very well matched.

A practical implementation of a phase splitter from a differential to a 4-phase signal is shown in Figure 3. The proposed phase splitter is well known and works well for wideband signals. The simulation results for the proposed phase splitter are shown in Figure 4.

Opportunities for improvement exist in all income groups. Low-income economies should focus on Internet access, mobile broadband penetration, and affordability. Middle- and high-income economies need to improve mobile broadband penetration and traffic per subscription.

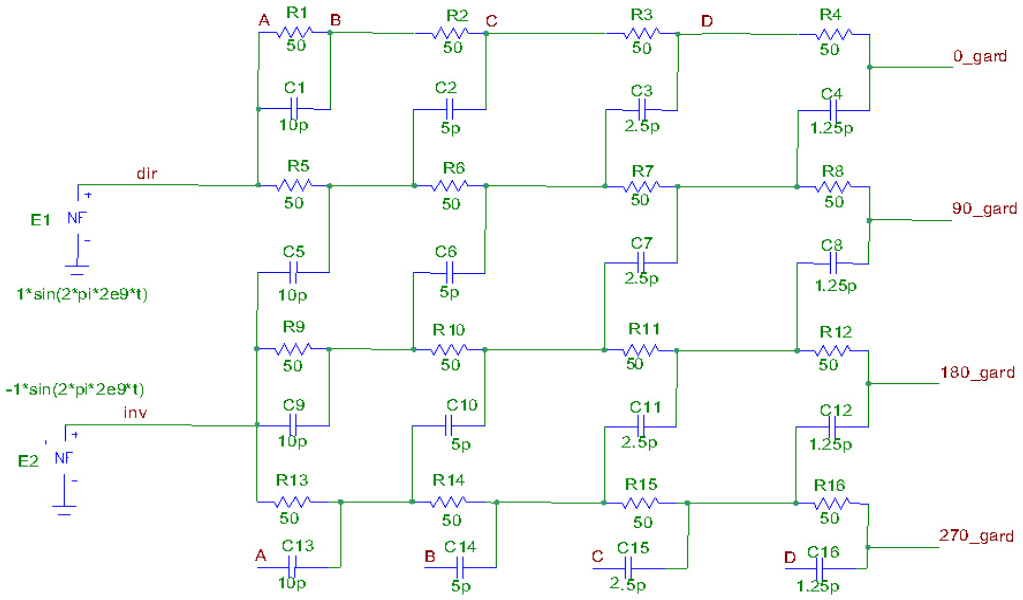


Fig. 3. Schematic implementation of a phase splitter from a differential to a 4-phase signal

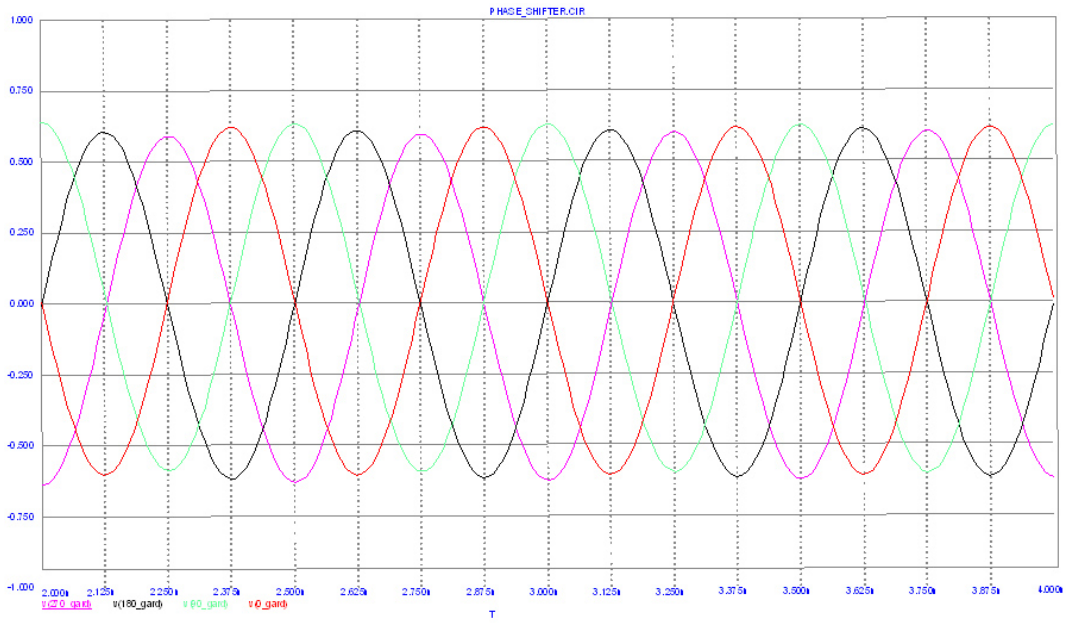


Fig. 4. Simulation results for the phase splitter

The following circuit can be proposed to convert the signal after phase shifting and attenuation to a differential output (Figure 5). Recommendations for the implementation of programmable attenuators are described in the following chapters.

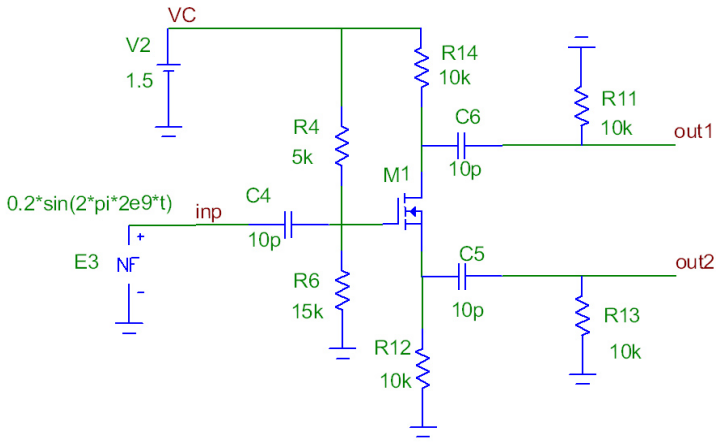


Fig. 5. Converter to differential output signals

3 Attenuator circuit implementation Examples

To implement the "Attenuator" and "Phase Shifter" blocks of the compensation circuit, an attenuator with a low noise level and a small parasitic phase shift when changing attenuation is required. Let us consider a resistive digital step attenuator, a P-I-N diode attenuator, and an active digital step MOS attenuator.

3.1 Resistive digital step attenuator.

A low-noise passive resistive digital step attenuator with a switch on MOS transistors (like the Microwave Office model) is shown in Fig. 6. The MOS transistor switch is considered as a combination of an ideal switch, an open-state resistor, and a parasitic output capacitor. The MOS transistor switches are ranked with the required resistance. The ratio of the on-resistance to the parasitic output capacitance is constant for all switches and equals 40 (example: R_{on} = 5 Ohm, C_{par} = 0.4 pF, X_{cpar} = 200 Ohm at 2 GHz). This ratio is modern for MOS technology.

The classic equation of the PI attenuator, allowing to calculate the resistance of parallel (R_{par}) and series (R_{ser}) elements:

$$R_{par} = R(A+1)/(A-1)$$

$$R_{ser} = R(A^2-1)/2A$$

where $A = U_{in}/U_{out}$ is the ratio of the input and output voltages.

To minimize the influence of switches parasitic parameters, some adjustments to the classic equation were used (after modeling and optimization):

R*par = 0.763*Rpar; Rsw_par = Rpar/5.8; R*ser = 1.218*Rser; Rsw_ser = Rser/21.1.

The results of the attenuation and parasitic phase shift analysis of the passive resistive digital step attenuator with a switch on MOSFETs are shown in Figure 7. The resistive digital step attenuator with a switch on MOSFETs has precision attenuation, but also has a large parasitic phase shift – more than 60 degrees. This circuit is not recommended for implementing the Attenuator and Phase Shifter blocks of the compensation circuit.

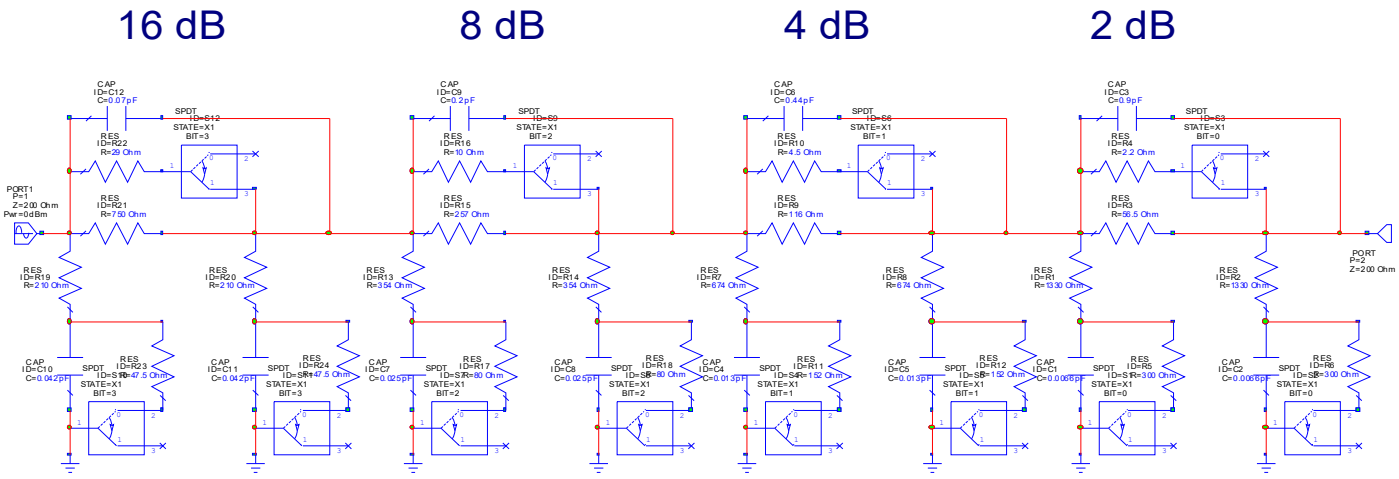


Fig. 6. Resistive digital step attenuator with a switch on MOSFETs (Microwave Office model)

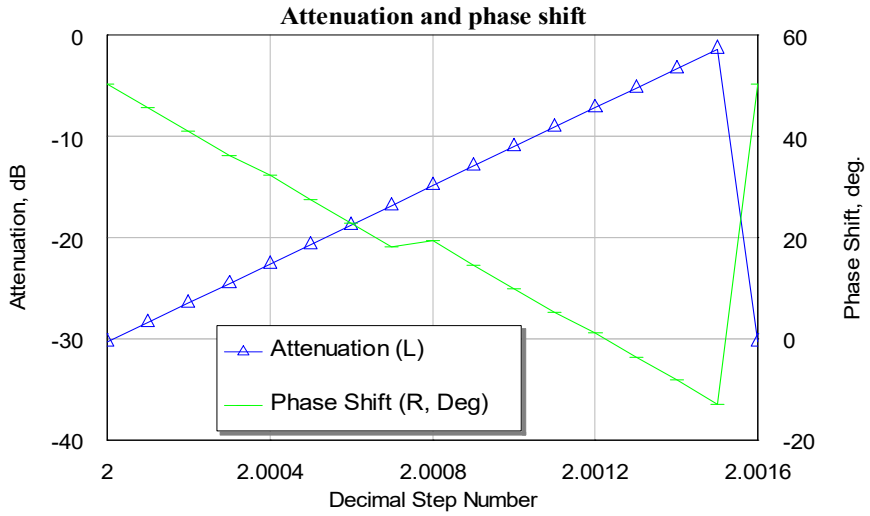


Fig. 7. Attenuation and parasitic phase shift of the passive resistive digital step attenuator with a switch on MOSFETs

3.2 P-I-N diode attenuator

The attenuator circuit based on a passive P-I-N diode [14] with a low noise level (as the Microwave Office model) is shown in Figure 8. PINDRC was used as an implementation of the Caverly PIN diode model. This advanced model is recommended for all types of PIN diode circuit design.

The equivalent circuit of the model is shown in Figure 9. The default parameters (Table 1) were used. The result of the analysis is shown in Figure 10.

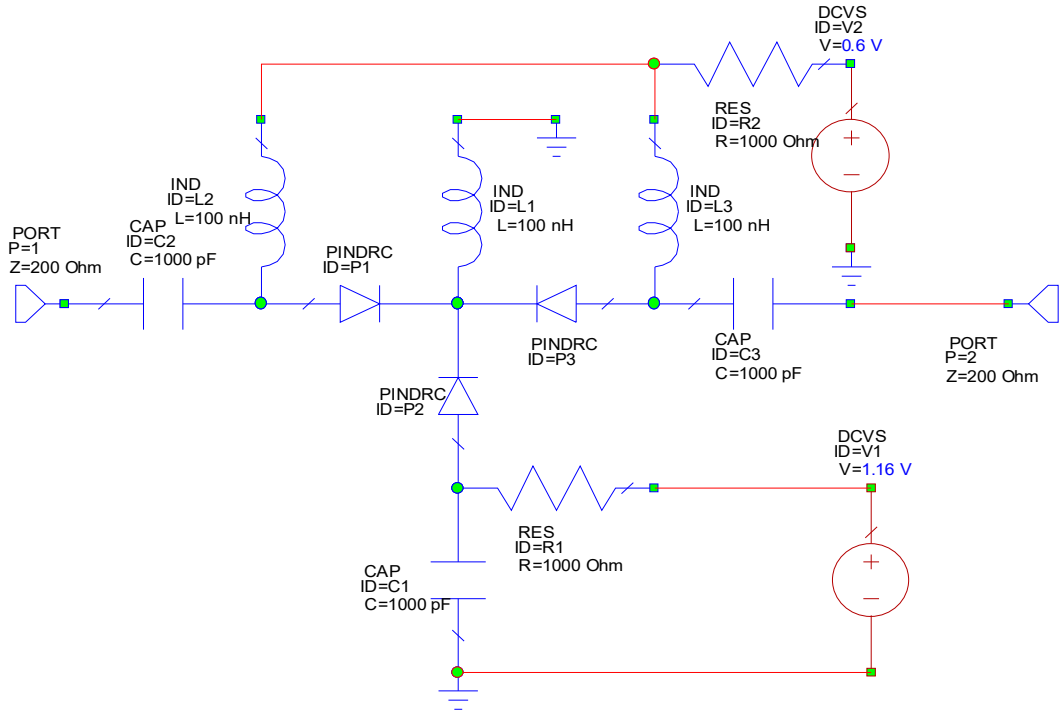


Fig. 8. P-I-N diode attenuator circuit (Microwave Office model)

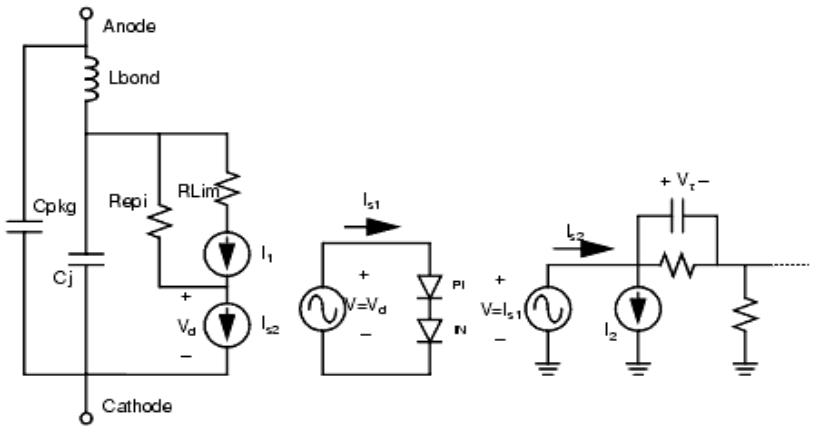
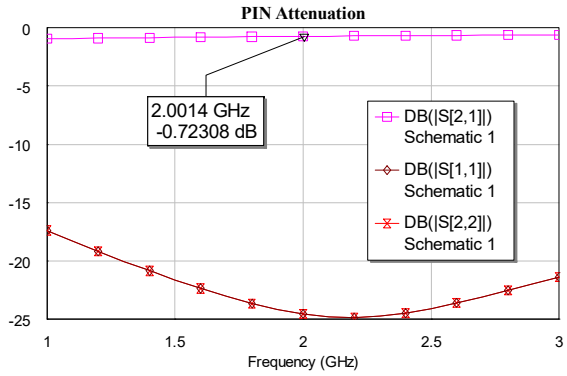


Fig. 9. Equivalent circuit of the PIN diode model

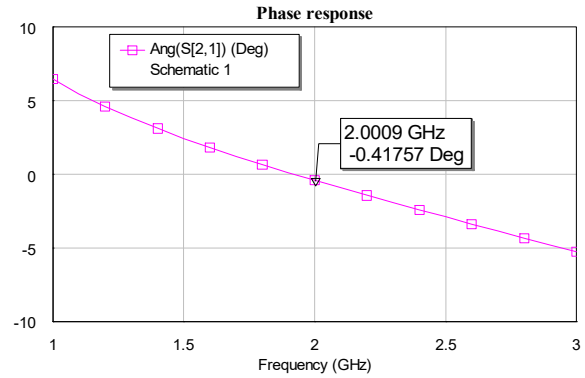
Table 1

PIN diode model parameters

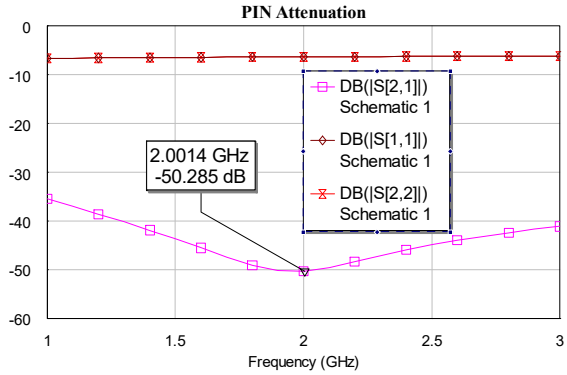
Name	Description	Unit Type	Default
ID	Device ID	Text	P1
IS	Reverse saturation current	Current	1e-6 mA
IKNEE	Knee param for current dependent tau	Current	1e6 mA
N	Ideality factor	Scalar	1
RLIM	Minimum series resistance	Resistance	0.001 Ohm
REPI	Epi leakage resistance	Resistance	1000 Ohm
CJ	Reverse capacitance	Capacitance	0.1 pF
CPKG	Package capacitance	Capacitance	0.1 pF
TAU	Storage time	Time	57 ns
W	I region width in micrometers	None	6.0 mm
B	Ratio of electron to hole mobility	Scalar	3.0
LBOND	Bond wire inductance	Indictance	0.1 nH



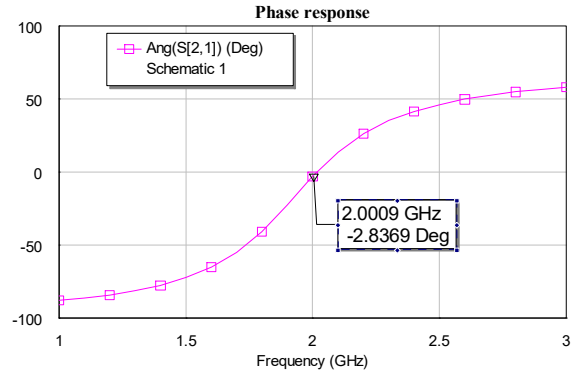
Minimum attenuation



Phase response at minimum attenuation



Maximum attenuation



Phase response at maximum attenuation

Fig. 10. Attenuator circuit on P-I-N diodes analysis results

The attenuator on P-I-N diodes has a wide attenuation range. For zero phase shift at any attenuation, precise matching of the current in the series and shunt path is required. The total current for all P-I-N diodes is about 4 mA at any attenuation - this is too much for the compensation circuit. Therefore, this circuit also cannot be recommended for implementing the Attenuator and Phase Shifter blocks of the compensation circuit.

3.3 Active digital step MOS attenuator

Two versions of the active step MOS attenuator are developed and considered. The first structure, shown in Figure 11, is based on the composition of weighted current sources. The four-bit part of the active digital step attenuator with the inclusion of MOS transistors is shown in Figure 11. The radio frequency signals from the resistive prescaler R1…R4 control four current generators implemented on NMOS transistors M1…M4 and resistors R18…R21. This allows to reduce the dynamic range of the scaling resistors. Thus, for an 8-bit attenuator, the range of resistor values is 16 instead of 256 without a prescaler. The output signal level is determined by NMOS switches in the sources of transistors M1…M4. Capacitors C17…C21 are installed to compensate for the parasitic phase shift. The power consumption of this circuit directly depends on the output signal level.

Since the real transistor model is not defined, a simplified model was used. The model includes nonlinear and noise characteristics of the transistor, but does not take into account the frequency characteristics. Therefore, the circuit shown in Figure 12 was used for the analysis.

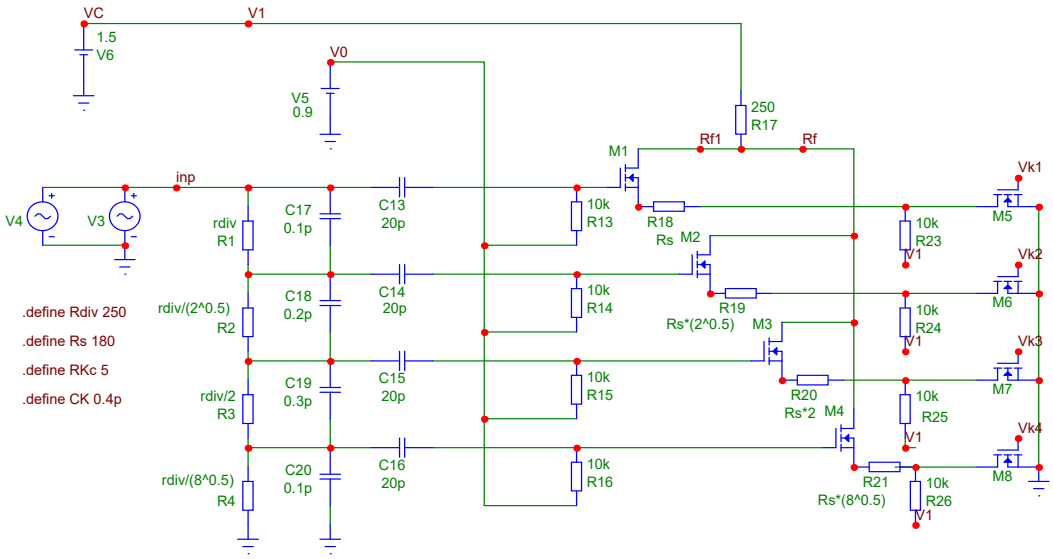


Fig. 11. Active digital step attenuator circuit (4-bit part)

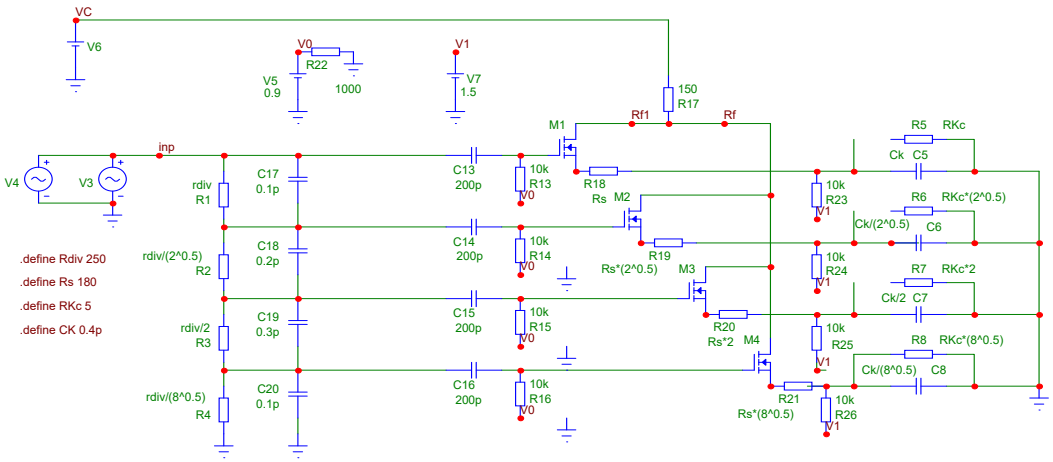


Fig. 12. Active digital step attenuator circuit model (4-bit part)

The real switches are represented by ideal switch with linear resistance and capacitance (R5…R8, C5…C8). The analysis results are shown in Fig. 13…16. The circuit has intermodulation distortions less than –40 dB on a two-tone test signal. The analyzed attenuator has a small parasitic phase shift and a low noise level. The high dynamic range allows installing a fixed attenuator and further reducing the output noise.

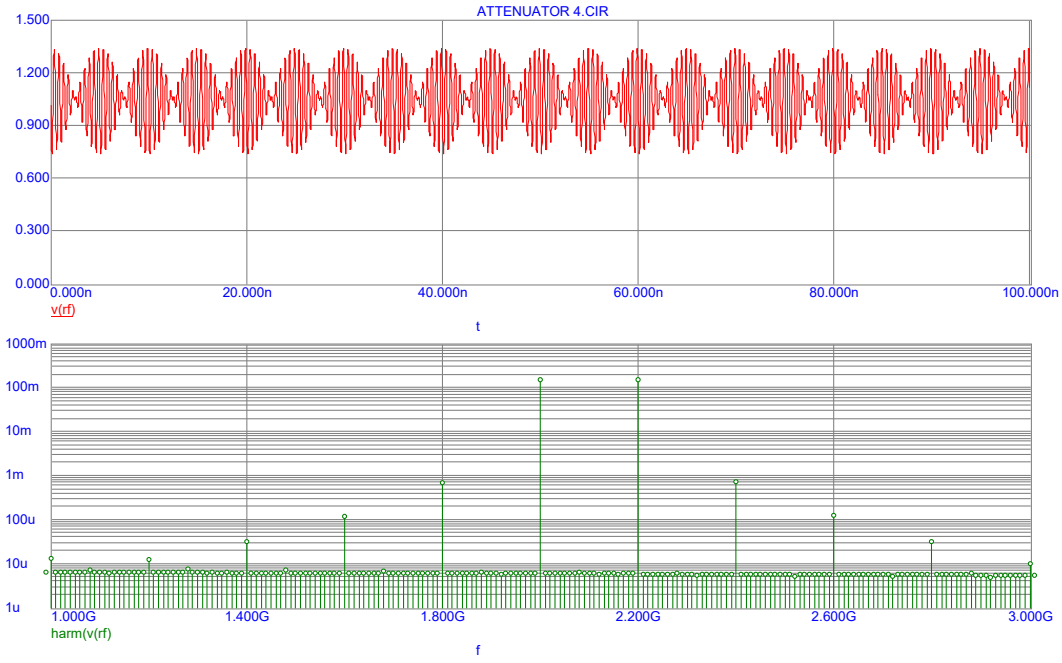


Fig. 13. Transient analysis result. Minimum attenuation

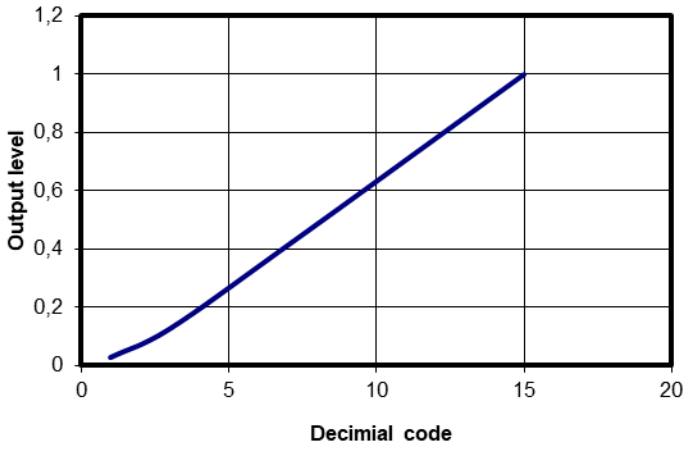


Fig. 14. Attenuator response

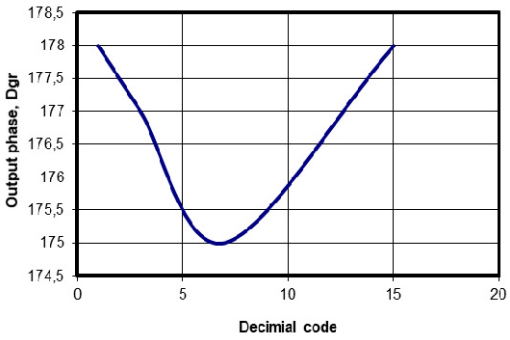


Fig. 15. Parasitic phase shift of the attenuator

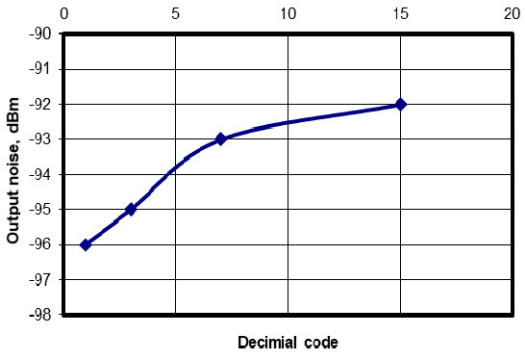


Fig. 16. Attenuator output noise, recalculated for a 50 ohm load

The second structure, shown in Figure 17, is based on weighted current summation. Switched current generators M3…M10 have different sizes based on the binary code. Switched transistors installed in the gate paths of the output transistors can be very small. Switched load resistors determine the scale range of the attenuator. The analysis results for this circuit are shown in Figures 18, 19. As can be seen, the circuit has a good dynamic range, but the output noise level seems too high over the entire possible current range. Therefore, this circuit needs noise optimization to be proposed for practical implementation.

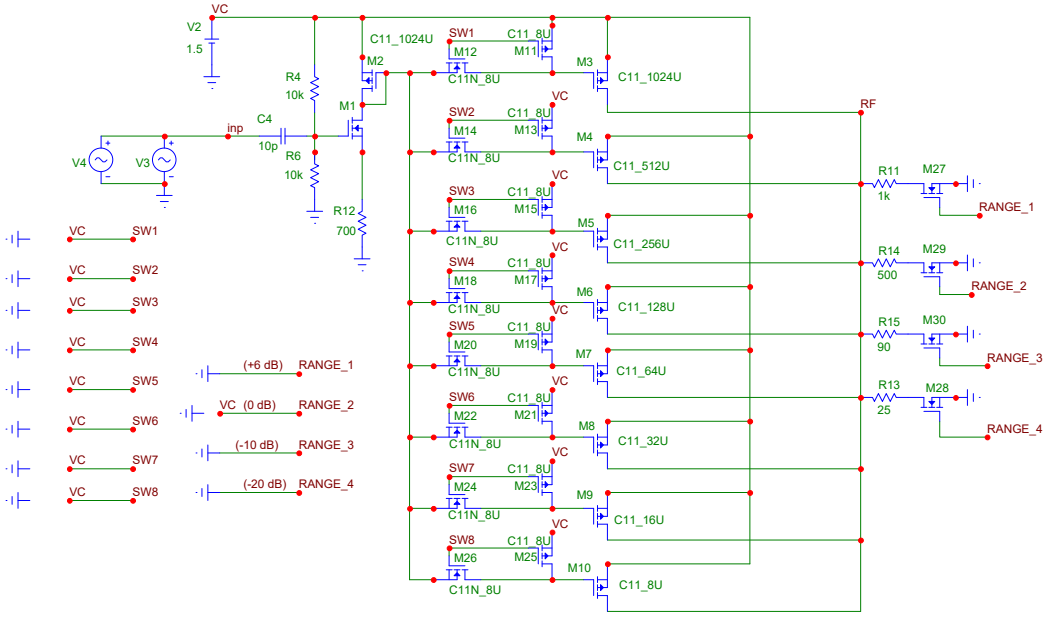


Fig. 17. Attenuator based on current summation

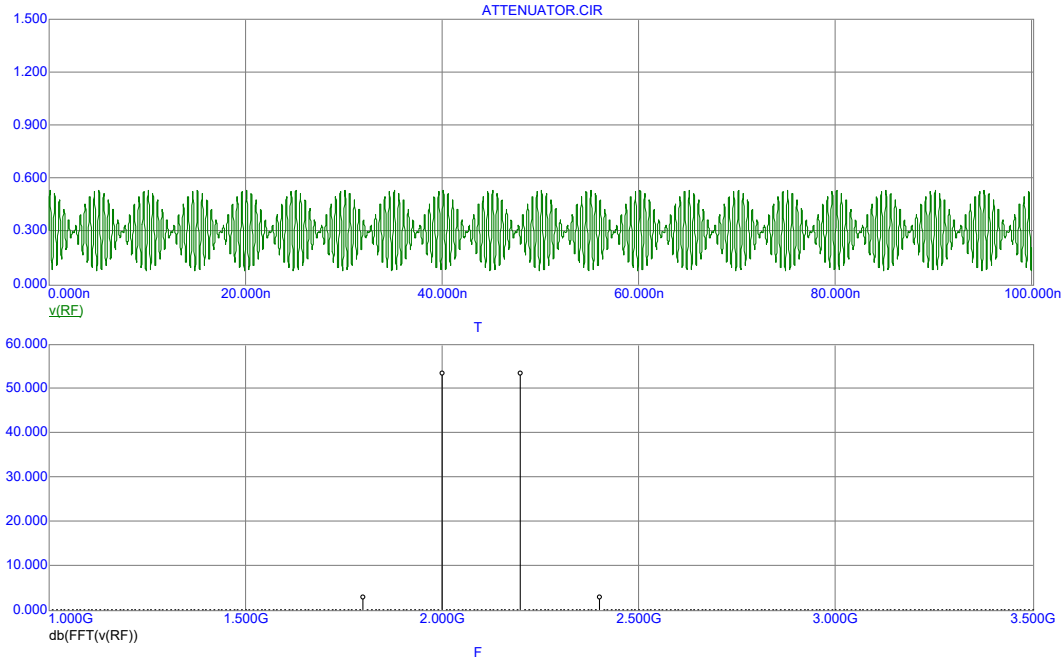


Fig. 18. Transient analysis result. Minimum attenuation

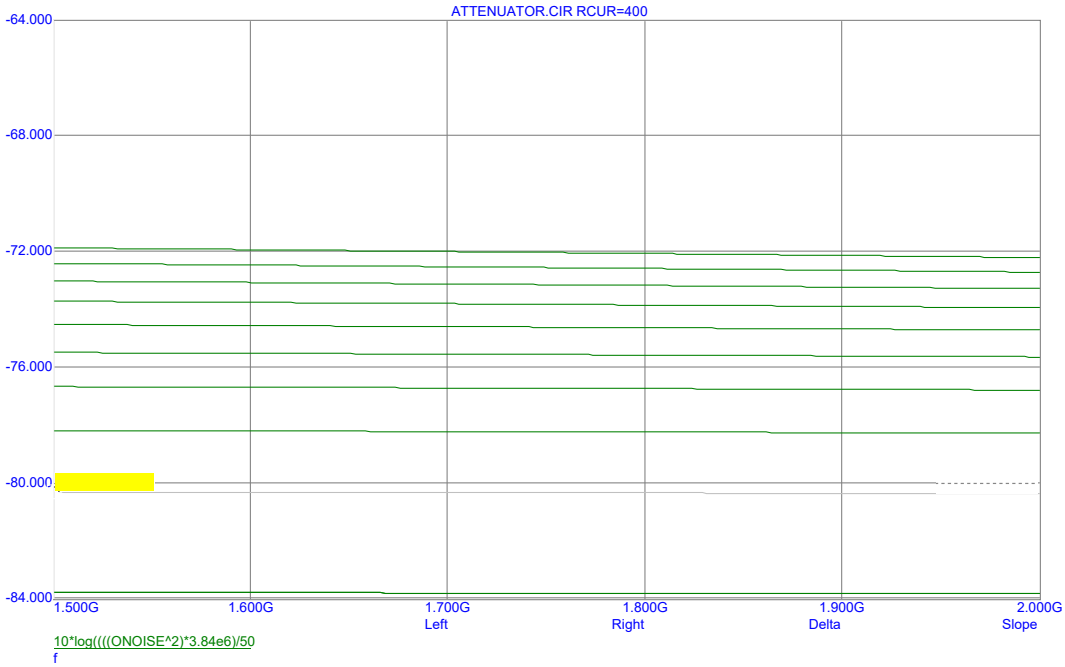


Fig. 19. Output noise power versus current control resistor value

Conclusion

The simulation of the considered implementation options for phase shifters and attenuators examples showed that:

– The resistive digital step attenuator with a switch on MOSFETs has precision attenuation, but also has a large parasitic phase shift – more than 60 degrees;

– The attenuator on P-I-N diodes has a wide attenuation range. For zero phase shift at any attenuation, precise matching of the current in the series and shunt path is required. The total current for all P-I-N diodes is about 4 mA at any attenuation – this is too much for the compensation circuit;

Both these circuits are not recommended for implementing the attenuator and phase shifter blocks of the compensation circuit.

– Active digital step MOS attenuator based on weighted current summation has a good dynamic range, but the output noise level seems too high over the entire possible current range. Therefore, this circuit needs noise optimization to be proposed for practical implementation;

– Active digital step MOS attenuator based on the composition of weighted current sources has intermodulation distortions less than –40 dB, a small parasitic phase shift and a low noise level. The high dynamic range allows installing a fixed attenuator and further reducing the output noise.

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